DSP Controlled Inverter Fed Speed Control of Three Phase Induction Motor

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Abstract

This paper describes the design of 3-Ø ac Induction motor drive with and without V/f control in open loop. It is based on Texas Instruments' TMS320C240 processor which is dedicated for Power electronic applications. Digital signal Processor is establishing cost effective and energy efficient control system design. The performance of DSP architecture allows an intelligent approach to reduce the complete system costs of digital motion control applications using cheaper electric motors, few sensors and small sizes of EMI filters. This DSP controller delivers the real time MIPS and the tightly integrated peripherals to implement optimal control algorithm with no cost penalty. The part is targeted towards the applications in both industrial and home applications such as washing machines, compressors, air-conditioning units, pumps or simple industrial drives. The software design takes the advantages of Software Development Kit developed by T.I. It adapts the principle of sinusoidal pulse width modulation technique for the generation of PWM signals to the Inverter module. This document includes basic Motor theory, system design concept, Hardware implementation and software design.

Keywords— DSPTMS320C240 processor architecture, **Event manager, GP (general purpose) timer, VSI, PWM generation and Induction motor.**

INTRODUCTION

Induction motors with squirrel cage rotors are the workhorse of industry because of their low cost and rugged construction. When operated directly from the line voltages, an induction motor operates at nearly constant speed. However power electronic converters are very effectively used to vary the speed of the motor. As explained in earlier section PWM inverter is an effective tool to control the speed of the motor by varying both voltage as well as frequency. By controlling the width of the PWM signals the voltage and frequency can be controlled. In the DSP processor there is a particular in-built module called EVENT MANAGER Module which is mainly used to generate PWM signals. The high frequency carrier wave is generated using up-down counter which is named as GP TIMER. The timer starts counting up until it reaches the maximum value which is specified in the program and from then it starts counting down until it reaches zero from which it starts counting up again which results in a repetitive triangular wave. From the above explanation it is clear that the carrier wave frequency depends on frequency of the clock input to the counter and the maximum value of the counter specified in program.

The angles at which intersection of the carrier wave and the modulating sine wave of desired frequency for one complete cycle of sine wave for the desired value of amplitude modulation ratio occurs are predetermined. The sine values at which both waves match are loaded into the data memory as a look-up-table. These values are regularly read when triangular wave reaches maximum and minimum values and loaded into a register called Compare register. Transition in the pulse occurs when the counter value matches with the value in compare register. The size of the look-up-table depends on the frequency modulation ratio. As the triangular wave and sine wave matches two times in each cycle of triangular wave sine wave matches two times the ratio of triangular frequency to sine frequency in a complete cycle of sine wave. The Optimization techniques which have been adapted for Microprocessor control can also be applied for DSP control. The output wave of the PWM inverter is of the sine wave. The frequency of the sine wave can be changed either by keeping the frequency modulation ratio (m_f) constant and by varying carrier frequency or by keeping carrier wave constant and by varying frequency modulation ratio (m_f). Both the above mentioned techniques have been implemented in the project. The output voltage of the inverter is varied by varying the amplitude modulation ratio (m_a). Both the frequency and voltage are simultaneously varied by keeping v/f ratio constant. In this paper a three phase sinusoidal PWM is generated using DSP for speed control of induction motor using voltage control, frequency control and v/f control. The voltage wave forms obtained from the three phase PWM inverter are 120^0 out of phase and able to run the induction motor satisfactorily.

DSP ARCHITECTURE

A functional block diagram of the 'C24X DSP controller architecture is shown in Figure a. The C24 x DSP architecture is based on a modified Harvard architecture, which supports separate bus structures for program space and data space. A third space, the input/output (I/O) space, is also available and is accessible through the external bus interface. To support a large selection of peripherals, a peripheral bus is used. The peripheral bus is mapped to the data space and interfaced to the data bus through a special system module. Thus all the instructions that operate on the data space also operate on all the peripheral registers. Separate program and data spaces allow simultaneous access to program instructions and data. For example, while data is multiplied, a previous product can be added to the accumulator, and at the same time, a new address can be generated. Such parallelism supports a set of arithmetic, logic, and bit-manipulation operations that can all be performed in a single machine cycle. The C24x also includes control mechanisms to manage interrupts, repeated operations, and function/subroutine calls

. EVENT MANAGER MODULE

In DSP TMS320F240, the Event Manager (EV) Module provides a broad range of functions and features that are particularly useful in motion-control and motor control applications. The block diagram of Event manager module is shown in Fig. B.

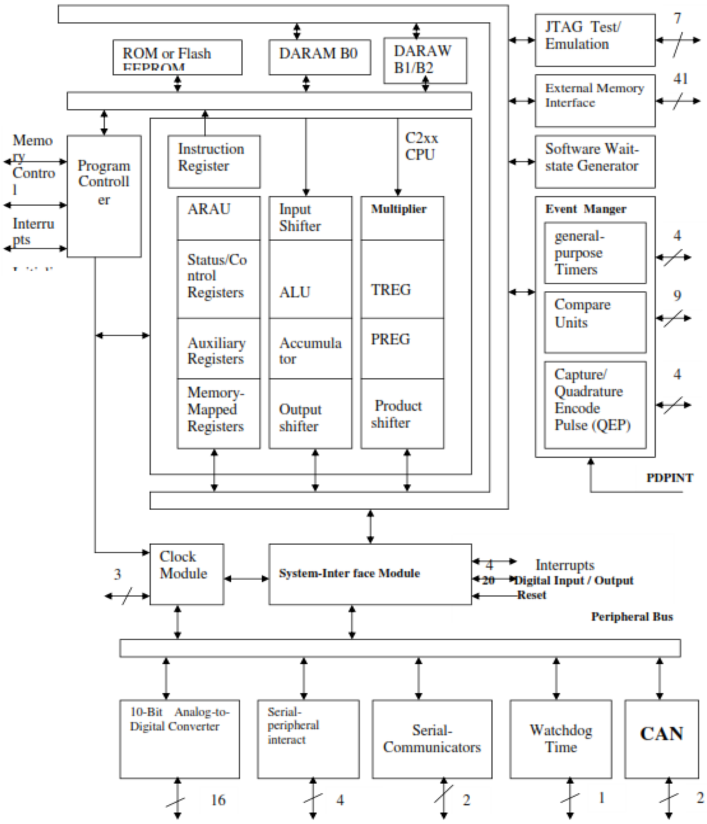


Fig a TMS320C 24X DSP Controller Functional Block Diagram

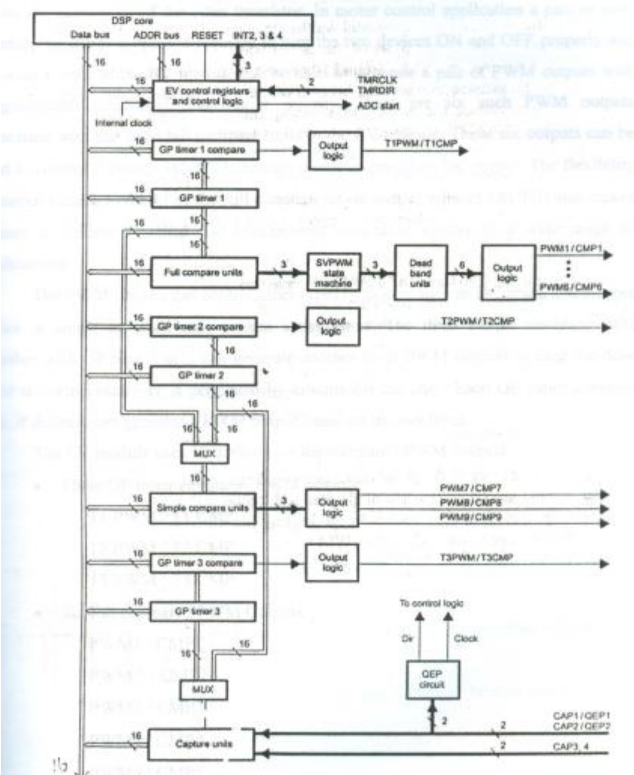


Fig. B Block diagram of Event Manager

The EV module contains

- Three general – purpose (GP) timers
- Three full compare units
- Three simple compare units
- Pulse Width Modulation (PWM) circuits that include
    i. A space – vector PWM circuit
    ii. Dead band generation units
    iii. Output logic
- Four capture units
- Quadrature encoder pulse (QEP) circuit
- EV interrupts

All registers in the EV module are mapped to data memory. Their addresses take up 64 (16-bit) words of the 64K words of data-memory address range.

PWM Signal Generation

To generate a PWM signal, an appropriate timer is needed to repeat a counting period that is the same as the PWM period. A compare register holds the modulating values. The value of the compare-register is constantly compared with the value of the timer counter. When the values match, a transition (from low to high or high to low) occurs on the associated output. When a second match is made between the values or when the end of the timer period is reached, another transition from high to low or low to high occurs on the associated output. In this way, an output pulse is generated whose ON or OFF duration is proportional to the value in the compare register. This process is repeated for each timer period with different modulating values in the compare register. As a result, a PWM signal is generated at the associated output.

Each of the three full compare units together with GP timer,1, the dead-band unit, a dead time (dead band) is often inserted between the turning off of one transistor and turning on of the other transistor. This delay allows complete turning off of one transistor before the turning on of the other transistor. In motor control application a pair of non-overlapping PWM outputs is required to turn the two devices ON and OFF properly and the output logic in the EV module can be used to generate a pair of PWM outputs with programmable dead-band and output polarity. There are six such PWM outputs associated with the three full compare units in the EV module. These six outputs can be used to control 3-phase (3ϕ)-AC induction motor or brushless DC motor. The flexibility of output behaviour control by the full compare action control register (ACTR) also makes it easy to control switched and synchronous reluctance motors in a wide range of applications.

The PWM circuits can control other types of motors such as DC brush and stepper motor in single or multi axis control applications. The three simple compare units together with GP time 1 or 2 can generate another three PWM outputs in case the dead band is not necessary or is generated by circuits off the chip. Each GP timer compare unit, if desired, can generate a PWM output based on its own timer. The EV module uses 12 device pins for compare / PWM outputs.

- Three GP timer compare / PWM outputs
    T1 PWM / T1 CMP
    T2 PWM / T2 CMP
    T3 PWM / T3 CMP
- Six full compare / PWM Outputs

PWM1 / CMP1
PWM2 ./ CMP2
PWM3 / CMP3
PWM4 / CMP4
PWM5 / CMP5
PWM6 / CMP6

- Three Simple Compare /PWM Outputs

PWM7 / CMP7
PWM8 / CMP8
PWM9 / CMP9

General Purpose Timers

There are three general purpose (GP) timers in the EV module. These timers can be used as independent time basis in applications such as:

- Providing the time base for the operation of full and simple compare units and associated PWM circuits to generate compare /PWM outputs.
- Generation of sampling period in a control system
- Providing a time base for the operation of QEP (Quadrature –Encoder Pulse) circuits and capture units.

Generation of PWM Output:

To generate a PWM output with a GP timer, select the continuous up counting or Up/Down counting mode. Edge-triggered or asymmetric PWM waveforms are generated when the continuous up counting mode is selected, centred or symmetric PWM waveforms are generated when the continuous up/down counting mode is selected. To setup a GP timer for the PWM operation, perform the following

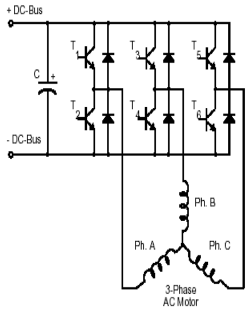
- Set up TxPR according to the desired PWM (carried) period
- Set up TxCON to specify the counting mode and clock source and start the operation
- Load TxCMPR with values corresponding to the on-line calculated widths (duty cycles) of PWM pulses.

When the continuous up counting mode is selected to generate asymmetric PWM waveforms, the period value obtained by dividing the desired PWM period by the period of the GP timer input clock and subtracting 1 from the resulting number. When the continuous up/down counting mode is selected to generate symmetric PWM waveforms, the period value is obtained by dividing the desired PWM period by 2 times the period of the GP timer input clock.

PWM INVERTERS

A Basic 3-φ Inverter is a six–step bridge inverter .It uses a minimum of six thyristors.For one cycle of 360°each step would be of 60° interval for a six step inverter. This means that thyristors would be gated at regular intervals of 60° in proper sequence, so that a 3-φ variable voltage is synthesized at the o/p terminals of six-step inverter .These are 2 possible patterns of gating the thyristors.

- 180° Mode of operation
- 120° Mode of operation



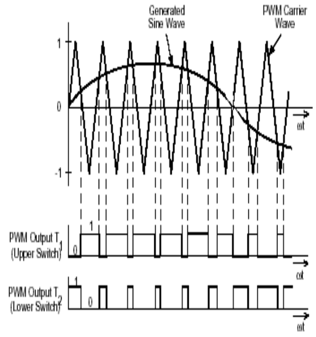


Figure 3-2. 3- Phase Inverter

1. **3-φ 120**$^\circ$ Mode **VSI:**

In this type of controls, each transistor conducts for 120° .Only two transistors remain on at any instant of time. It is seen that phase voltages have one +ve pulse and one –ve pulse each of duration 120°.the line voltages have sin steps/cycle of output alternating voltage.

$$Va_0 = \sum_{n=1,3,5}^{\infty} \frac{2Vs}{n\Pi} \cos\frac{n\Pi}{6} \sin n(wt + \frac{\Pi}{6})$$

$$V_{ab} = \sum_{n=6R\pm1}^{\infty} \frac{3Vs}{n\Pi} \sin n(wt + \frac{\Pi}{3}) \text{, where R=0,1,2, 3…}$$

PWM Inverters are gradually taking over other types of Inverters. In these forced commutation is essential. In pulse width modulation a control voltage control is compared with repetitive switching signals. Controlling the switch duty ratios in this way allowed the average dc voltage output to be controlled.

In order to produce sinusoidal output voltage waveform at desired frequency a sinusoidal controls signal at a desired frequency is compared with a carrier wave. The frequency of the carrier waveform establishes the inverter switching frequency and is kept constant along with its amplitude.

Amplitude Modulation Ratio (m_a) = $\frac{V_{control}}{Vtri}$

Frequency Modulation Ratio (m_f) = f_s/f_1.

For generating PWM pulses DSP processor is used to generate sinusoidal voltage of desired magnitude and frequency. In this modulating signal is stepped wave. The stepped wave is not a sampled approximation to the sine wave. It is divided as shown in fig.c this type of control gives low distortion, but higher fundamental output amplitude compared to that of normal PWM control.

Design Considerations:-

Amplitude Modulation ratio:-

Though over modulation region compared to the region with ma<1.0, more sideband harmonics appear centered around the frequencies of harmonics mf and its multiples. It is preferred for motor control applications as higher voltages can be obtained.

Frequency Modulation Ratio:

a) m_f should be an odd integer:- choosing m_f as an odd integer results in an odd symmetry [f(-t) = -f(t)]as well as half wave symmetry [f(t) = -f(t+Ts/2)]and Hence all even harmonics disappear from waveform & only odd harmonics are present .Moreover only coefficients of sine series in the Fourier analysis are finite & those for cosine series are zero.

b) m_f should be multiple of 3: Choosing m_f value such that it is a multiple of 3 results in elimination of triple harmonics.

c) m_f should be an integer: choosing an m_f value as an integer especially at low value of m_f's results in synchronous PWM which avoids production of sub harmonics. For small values of m_f ($m_f \leq 21$)

(i) Synchronous PWM should be used.
(ii) m_f should be an odd integer.
(iii) Slope of $V_{control}$ & V_{mi} should be of opposite polarity at the coincident zero crossings.

Hence by considering all the above facts m_f is chosen as '15':

Carrier frequency:-

Because of the reactive case in filtering harmonic voltages at high frequencies, it is desirable to use a high switching frequency as possible, but at the same time switching losses in the inverter increase proportionally with switching frequency. In most applications f_s is selected to be either less than 6 KHz or greater than 20 KHz to be above the audible range.

Hence it is chosen as 750Hz.

Synchronous & Asynchronous PWM:-

The triangular wave form signal control signal should be, synchronized to each other (synchronous PWM). Otherwise asynchronous PWM results in sub harmonics that are very undesirable in most applications. Synchronous pwm can be obtained by choosing integer values of mf.

Symmetric & Asymmetrical PWM:-

PWM signal is symmetric if the signal is symmetric around the period value. Symmetric PWM is generated if the carrier wave is triangular & asymmetric pwm generated if saw tooth wave is chosen as carrier wave. Generally symmetric PWM is used

SPEED CONTROL OF INDUCTION MOTOR

In a large majority of applications induction motor drive incorporates a 3-ø Squirrel cage motor. Hence the speed control techniques of the motor are very important aspect to be concentrated on. The objective of this section is to discuss the speed control techniques of the motor and their effects on the performance of the motor.

Variable Voltage Operation

On a 50 Hz fixed frequency the torque developed by the induction motor, at a given slip, varies approximately as square of the applied voltage. And the continuous speed control is obtained by step less adjustment of stator voltage without any alteration in the stator frequency. Stator voltage control eliminates the complex circuitry for speed control of motor and cheaper to install. However operating frequency is poor. And motor must be derated at low speeds. During light loads, this control technique reduces the power consumption by applying reduced voltage.

Constant torque load:

The power transferred from stator to rotor is

$$P_g=E_2I_2\cos\theta_2$$

Electromagnetic torque $T_e=E_2I_2\cos\theta_2/\omega_s$

The supply voltage is related with the flux as $V_1= 4.44*f*N_1 *\phi* k_w$

If supply voltage decreases to V_2 for constant load torque, the slip for voltage V_1 increase to slip s_2 for voltage V_2. With the increase in slip, rotor power factor also decreases. Since both ø and cos Θ_2 have decreased for reduction in supply voltage, for a constant load torque rotor current I_2 must increase and hence rotor ohmic losses increases. Here though magnetizing current decreases supply current equal to the phasor sum of I_2 and $I_ø$ becomes more.

If supply voltage increases, the operating slip would decrease very slightly and likewise the rotor power factor would be improved by a small value. Since the flux increases with the increase in voltage, the magnetizing current increases and rotor current decreases for constant load torque. If the increase in supply voltage is large, the increase in magnetizing current would more than compensate the decrease in I_2 and consequently the supply current would increase. The increase in supply current would result in motor overheating.

Constant power load:

The mechanical power developed in a 3-ф I.M is

$$P_m= (1-s)\ P_g = (1-s)\ I_2^2r_2/s$$
$$= (1/s-1)\ I_2^2r_2$$

If the supply voltage decreases the operating slip increases for constant power load. From the equation I_2 must increase for an increase in slip. Hence the effects with the reduction in voltage are more ohmic losses, low operating speed, less efficiency, more temperature rise and lower operating life.Similarly with the increase in supply voltage is accompanied by an increase in $I_ø$ and hence the increase in supply current of induction motor driving constant power loads.

Variable Frequency Operation:

Modern methods of static frequency conversion have liberated the induction motor from its historical role as a fixed-speed machine, but the inherent advantages of adjustable-frequency operation cannot be fully realized unless a suitable control technique is employed. Open loop speed control of an induction motor with an adjustable –frequency supply provides a satisfactory adjustable-speed drive when the transient performance characteristics are undemanding and the motor operates at steady speeds for long periods If supply frequency varies, the flux gets changed and so the magnetizing current. A decrease in frequency means greater flux and also a larger magnetizing current. The large value of flux may cause saturation of the motor magnetizing circuit.

Constant – torque load:

A decrease in frequency means greater air-gap flux, lower X_2, and hence the power factor increase slightly which in turn requires less value of I_2. On the other hand with the increase in flux the magnetizing current increases, which may overcompensate the decrease in I_2 and therefore the supply current, may increase, likewise the motor power factor may be worsened instead of improving. Thus a decrease in frequency with constant V and T_L means lower operating speed, decreased motor output, better starting and pull-out torques and operating power factor may be improved or worsened depending upon the increase in ø.

Constant power load:

A decrease in frequency means, lower operating speed. Consequently constant-power load requires greater electromagnetic torque. The operating power factor, with the decrease in frequency improves and for a constant $V_1I_1\cos\Theta_1$, supply current decreases. Depending upon the decrease in frequency and, therefore on the increase in the air gap flux, the magnetizing current increases which may tend to compensate the decrease in supply current. This shows that a decrease in frequency with constant power load means lower operating speed, greater electromagnetic torque and a decrease in supply current may be under compensated or over compensated by an increase in the magnetizing current.

Constant V/F Operation.

If supply voltage and frequency are changed in such a manner so as to keep V/f a constant value, then the air-gap flux remains substantially constant. Speed control by means of frequency and voltage variations also allows the capability to operate the motor not only at speeds below the rated speed, but also above the rated speed. This capability is very attractive in many applications, since the induction motors can be operated up to twice the rated speed without mechanical problems.

Below The Rated Speed—Constant Torque Region: In the region of speed below its rated value, where øag kept constant by controlling Vs/f. if $ø_{ag}$ is maintained constant, and the motor can deliver its rated torque by drawing its rated current at a constant f. Hence this region is called as constant torque region .F is at its rated value in this region. At the constant rated torque, the power loss $P_r=3R_rI_r^2$ in the rotor resistances also constant, where I_r stays constant.

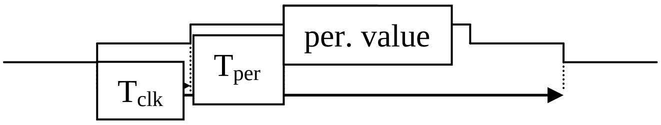
Beyond The Rated Speed ----- Constant Power Region.

By increasing the stator frequency above its nominal value, it is possible to increase the motor speed beyond the rated speed .in most adjustable speed drive applications; the motor voltage is not exceeded beyond its rated value. Therefore by keeping the Vs at its rated value, increasing the frequency F results in a reduced Vs/F and, hence by reduced $ø_{ag.}$ Hence this region $P_{max}= \omega_r T_{max}$ can be held constant , called as constant power region. In practice, the motor can deliver higher than its rated power by noting that I_m goes down as a result of decreased $ø_{ag \text{ and therefore is equal to its}}$ rated value allows a higher value of I_r and, higher torque and power. Since I_m is decreased, the core losses are reduced and better cooling at higher speeds.

PROGRAMMING TECHNIQUES

This section describes the Algorithm, flow chart and programming techniques for the generation of 3-Ø sinusoidal PWM signals. The pulses obtained from the corresponding Algorithm and program, are tested with IPM inverter module. The output of the inverter module is given to induction motor. The speed of the motor is controlled by varying width of the pulses as well as the no of pulses per cycle.

Calculation of Period value and Compare value:



Referring to the above figure it is clear that the carrier frequency holds a proportional tic relation with the period value. The value of the period value determines the carrier frequency at constant clock frequency. Since the GP timers start counting from zero, to calculate the value that should be loaded into the period resister, one should be subtracted from the calculated value obtained to input into register T1PR. As the GP timer counts up and then count down the period value is given by PER. value= $T_{car}/ (2 * T_{clk})$

= Clock frequency/ (2 * desired carrier frequency)

= (CLK infrequency * PLL multiplication Ratio/PLL divided by 2) Pre scale value* desired carrier frequency.

Here the pre scale value is 2 for triangular wave & 1 for saw tooth wave_Compare value = (period value/2)* duty cycle. For obtaining PWM signal, the program is written in Standalone mode. In this mode, the registers are identified by their address values.

Creating a sine modulated PWM signal using the micro-240:

A Symmetrical sinusoidal pulse width modulation (PWM) signal is generated with a varying duty cycle. The duty cycle is modulated with a sine function that can be varied in frequency. The implementation of the sin wave modulation is through a look-up table using C240 assembly code. The module used to generate the sine PWM signal is the general purpose time of the event manager module. Although the primary module is the event manager module, other components of the TMS320c240 need to be configured prior to the generation of sinusoidal PWM signals.

Generation of 3-Ø sinusoidal PWM signals:

For the generation of 3- Ø sinusoidal signals the sine wave of desired frequency is continuously compared with high frequency triangular wave. The angles where the two waves match are found using C code. These values are loaded into the processor as a look-up-table.

The triangular wave of desired frequency is generated using GP Timer. The frequency of the triangular wave is determined by the value in Period register. The sine of the angles at which compare match occurs are loaded in Q15 format in the look-up-table. The counter value will always be a positive value. In order to account the negative compare matches the reference is shifted by adding the reference value to the sine values. The sine values are retrieved from the look-up-table every time the underflow (when the timer value becomes zero) or Period match occurs. The sine values are multiplied with the amplitude value to get $V_m \sin\theta$. Reference value is then added to the obtained value and stored in Compare register. The reference value is half the period value. The 3-Ø signals are obtained by pointing the respective phases with 120° phase shift in the look-up-table.

For changing the output voltage the value of V_m is changed. For varying the output frequency either the carrier frequency can be changed by changing the period value or by changing the frequency modulation ratio (m_f) by producing time delay while loading the value into compare register. For V/f control both the voltage and frequency is varied by controlling the m_a and m_f value using the above mentioned methods.

The value of V_m to be loaded is found by the relation

$V_m = m_a * (\text{period value}/2)$

And the reference value is given by period value/2.

Algorithm:-

1. configure the flags
   - All the interrupts are disabled and core interrupts are masked
   - Read interrupt flags and clear the flags
   - Clear sign extension mode and reset the overflow mode
2. The CPU clock speed is set to a maximum of 20MHz. The PLL is enabled for this purpose.
3. The watch dog timer is disabled since it is not necessary for application.
4. Since the event manager module is used in the program, the following steps are performed.
   - General purpose timer control (GPTCON), GP timer 1, 2, 3 (T1CON, T_2CON, T3CON) are all cleared.
   - Compare control (COMCON), Full Compare action control, simple compare action control, Dead-band timer control (DBT CON) and capture control are all cleared.
   - All the interrupt flag registers A,B,C and three event manager mask registers are cleared
5. declaration of temporary variable :
   - temporary variables for PWM 1 and2, PWM 3 and 4, PWM 5 and6 are declared,
   - Temporary variables for ADC values are declared.
   - Since, variations in amplitude and frequency are needed, variables for freq value and amp value are declared.
   - Counters for increase and decrease of values are declared as up button counter and down button counter
6. The GP timers 1 period interrupt and under flow interrupt flags are enabled. The ACTR is configured for all the six PWM outputs PWM1, 3, 5 are made active high and PWM2, 4, 6 are made active low.
7. The DBTCON register is configured for 18 fs and 5fs dead band generation
8. The GPTCON register is configured such that timer2 is active high for fault generation.
9. Using COMCON registers configure for full compare outputs and check for enable

10. The GP timer 1 period register is configured for generating 750Hz carrier signal. The GP timer1 control register is reset. Configure the GP timer1 control register in up/down counting mode and enable the timer 1.
11. A 3-Ø inverter requires PWM signals with 120^0 phase shift. So the phase shift index value is set at 120° and 240º with respect to the first carrier wave.
12. Select the ADC channels. Store the length of sine table for PWM 5 and PWM 6, PWM 3 and PWM4 and PWM1 and 2 in the respective auxiliary registers 5, 4, 3 and their pointers in auxiliary registers 2, 1, 0.
13. Load the frequency and amplitude in the temporary variables.
14. Configure the general purpose I/O pins.
15. Check SPDT switch is 0. If yes the update1 routine is executed, else update routine is executed.
16. Update 1 routine checks whether up button is pressed. It yes, it increments up button counter 1 and increases the amplitude. Else it checks for down button and some process takes place except for that, it decreases the amplitude.
17. Update routine check for up/down button press. It increments the respective up/down button counter and decreases /increases the frequency respectively.
18. Check for proper dead band generation for PWM1 and 2, PWM3 and 4 and PWM 5 and6.
19. Manipulate Q15 values and place in compare registers
20. Since, the PWM 3 and 4 are generated at 120^0 phase shift form PWM1 and 2, the compare value is not incremented till 120^0 position of table is reached. Similarly PWM 5 and 6 are generated only after 240^0 phase shift from PWM 1 and 2.
21. Each time the table values are incremented and when end of table is reached, the table is re-loaded, the table is reloaded and process continuous.
22. For fault generation, timer 2 is enabled. The ADC values are input and compared with the set value, if it exceeds the value,
    fault generation timer 2 is enabled and all the COMCON register is disabled, so that no PWM is generated.

TESTS AND EXPERIMENTAL RESULTS

1) VOLTAGE CONTROL: (Frequency constant)

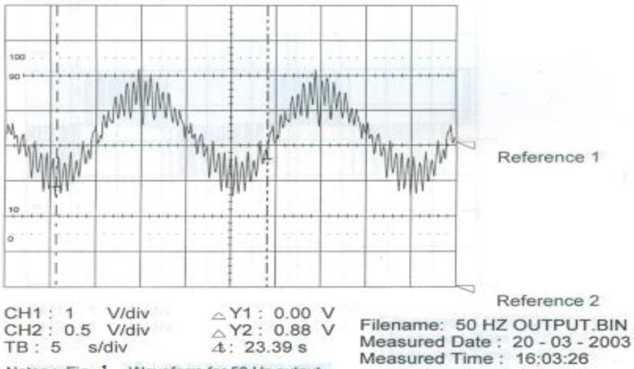
S.NO	m_a (In hexa)	$V_{D.C}$ (Volts)	$V_{a.c}$ (Volts)	$I_{a.c}$ (amps)	SPEED (r.p.m)
1.	41A9	600	400	1.0	1440
2	3BB0	600	380	1.0	1435
3.	372B	600	360	1.0	1435
4	3227	600	340	1.0	1435
5	2C18	600	320	1.0	1435
6	269C	600	300	0.8	1435
7	2288	600	280	0.7	1430
8	1E88	600	260	0.6	1428
9	1A87	600	240	0.5	1428
10	1515	600	220	0.2	1425
11	1125	600	200	0.2	1410
12	0DAB	600	180	0.1	1390
13	09BF	600	160	0.1	1360
14	0632	600	150	0.1	1340
15	04EF	600	144	0.1	1260
16	0485	600	140	0.1	1180
17	02F1	600	120	0.1	150

2).FREQUENCY CONTROL: (FIXED m_a =1.0)

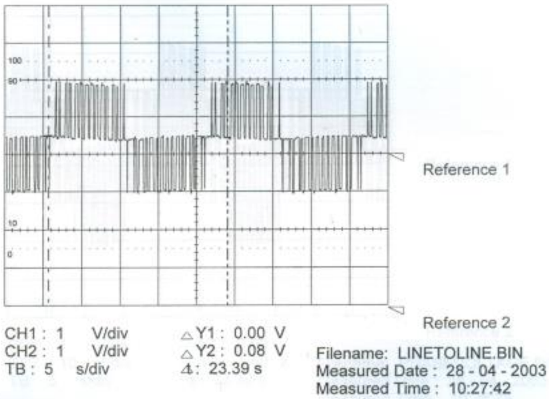
S.NO	$V_{d.c}$ (const)	m_f	$V_{a.c}$ (volts)	Frequency (Hz)	Speed (r.p.m)	$I_{a.c}$ (amps)
1.	620	0000	400	50	1440	1.2
2.	620	00F0	400	48	1436	1.2
3.	620	053C	400	46	1398	1.2
4.	620	0577	400	44	1320	1.2
5.	620	05C6	400	42	1240	1.2
6.	620	0616	400	40	1150	1.2
7.	620	3050	400	52	1550	1.2
8.	620	2DFC	400	55	1615	1.2

3).V/F CONTROL :

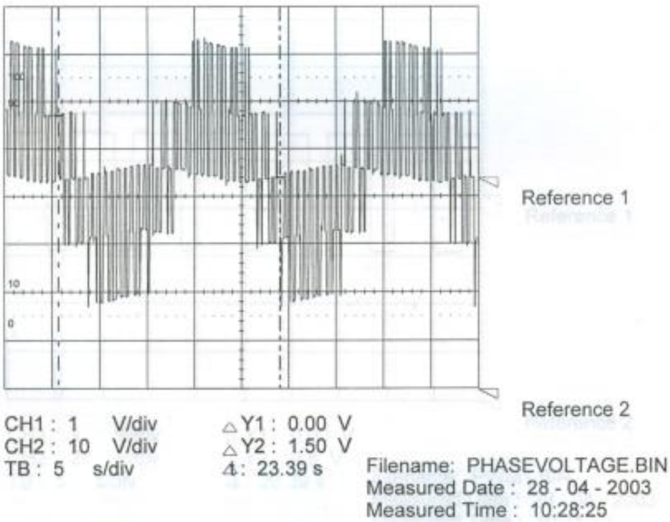
S.NO	$V_{d.c}$ (const)	m_a	m_f	$V_{a.c}$ (volts)	Frequency (Hz)	V/F	Speed (r.p.m)	$I_{a.c}$ (amps)
1.	620	4239	0000	400	50	8	1440	1.2
2.	620	3B83	0F00	384	48	8	1440	1.2
3.	620	47AE	053C	368	46	8	1400	1.15
4.	620	4621	0577	352	44	8	1340	1.15
5.	620	43FE	05C6	336	42	8	1270	1.15
6.	620	3CE1	0616	320	40	8	1200	1.1
7.	620	4F15	3050	416	52	8	1550	1.1
8.	620	3D41	2DFC	440	55	8	1610	1.1



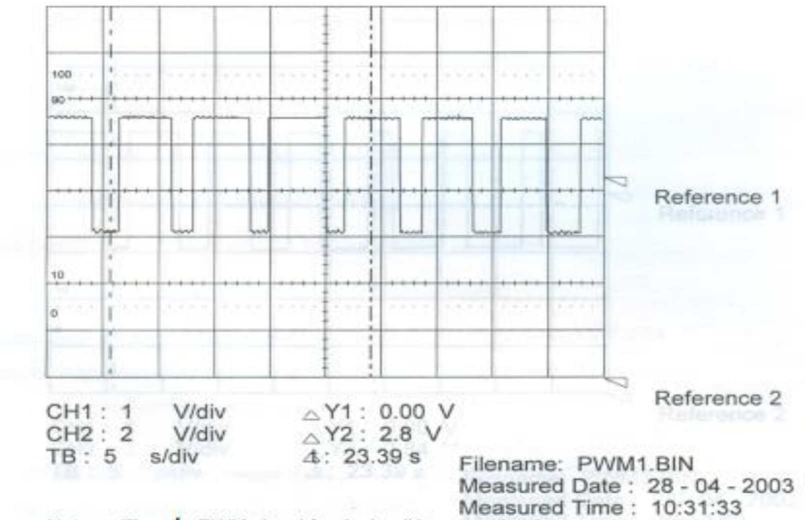
Notes : Fig. 1 Waveform for 50 Hz output



Notes : Fig.2 Line to line voltage waveform for 50 Hz output



Notes : Fig. 3 Phase voltage waveform for 50 Hz output



Notes : Fig. 4 PWM signal for device #1

CONCLUSIONS

The sinusoidal PWM signals are generated using the DSP processor (TMS320C240) and the signals are given to inverter module. The 3-ф output from the inverter module is given to 3-ф induction motor and speed of the motor is controlled with and without V/F control. The high speed architecture and flexible characteristics of the processor made the speed control of the motor most effective compared to other conventional techniques. The motor is made to run above and below base speed. The proper designing of PWM inverter parameters minimised the harmonic content. The readings of speed, supply current and voltages have been taken for various speed control techniques. The waveforms of PWM pulses, line and phase voltages as well as currents have been taken. An improved dynamic response is obtained and this method is recommended for speed control of industrial drives as well as home applications.

REFERENCES

1. J.M.D MURPHY and F.G.TURNBULL-power electronic control of AC motors.
2. NED MOHAN,TORE M.UNDELAND and WILLIAM P.POBBINS-power electronics converters, applications and design.
3. Power semiconductor controlled drives-Gopal.K.Dubey.
4. MICRO-240 USER manual version 2.0 Microsystems Pvt.Ltd.Chennai.
5. MICRO-240 Technical Reference version 2.0, Vi Microsystems Pvt.Ltd.chennai.
6. TEXAS INSTRUMENTS TMS 320F/C 24 x DSP controller- CPU and instruction set (reference guide).
7. TEXAS INSTRUMENTS TMS 320F/C 24 x DSP controller-Peripheral library and specific devices (reference guide).
8. Trzynadlowaki, A.M.Kirlin and Legowski.s.f “space-vector PWM technique with minimum switching losses and a variable pulse rate;”IEEE transctions on industrial electronics, vol. 44, No.2, April 1997.