Realistic implementation and validation of a Macrocell /Femtocell Interference-mitigation Technique for LTE-based systems

A.M. Bharath Kumar

Asst.Professor,Dept of ECE,Krishna chaitanya Institute of Technology and Science, Markapur,Prakasam(Dist),Ap,India.e-mail: mamidi436@gmail.com

***Abstract*—**This paper provides details of the design, implementation and realistic verification of a macrocell/femtocell interference-mitigation technique targeting high-performance broadband LTE-based wireless communication systems. As in the Existing methods, the focus is laid on the description of the FPGA design and the employed RTL techniques, whose goal was to provide a hardware-efficient implementation of adaptive PHY-layer solutions. An important aspect of the presented PHY-layer prototyping is the utilization of real-life operating conditions, hardware specifications, constraints and mobile channel propagation conditions. In order to support the complex development cycle it was introduced an iterative design, implementation and verification methodology, covering all the required steps from the definition of the system requirements and high-level modelling to the comprehensive evaluation of the resulting prototype based on a realistic hardware-setup. Two representative use cases detail this core contribution and underlined the suitability of the proposed development flow. The first use case is a 2x2 MIMO closed-loop PHY-layer scheme, based on the mobile Worldwide Interoperability for Microwave Access (WiMAX) wireless communication standard and featuring a Transmit Antenna Selection (TAS) mechanism. The second use case implements a 3rd Generation Partnership Project **(3GPP) Long Term Evolution (LTE)-based macrocell/femtocell interference-management scheme.**

Keywords **Macrocell /Femtocell , PHY layer, OFDMA**

1. Introduction

The designated RF spectrum of modern cellular-based wireless communication networks is every time more congested, whilst requiring to serve an increasing number of users (i.e., mobile and fixed). The RF spectrum reuse has been proposed as one of the key technology drivers for the deployment of next generation BWA systems. The efficient deployment of the previous scheme constitutes one of the main goals of CR. However, the opportunistic reuse of the RF spectrum requires the agile mitigation of the effects caused by in-band interfering RF signals. Interference management is therefore becoming an indispensable feature that has to be accounted throughout the joint design of the PHY and MAC layers of network infrastructure equipment, Customer Premises Equipment (CPE) and mobile User Equipment (UE). Two major interference management categories can be found in the literature. The first one includes interference avoidance techniques such as spectrum sensing, aiming at the instantaneous allocation of unused-unlicensed spectrum. The second one encapsulates interference mitigation schemes that enable high spectral efficiency through frequency reuse, i.e., the same frequency bands are used by different users among adjacent (heterogeneous) cells. An indicative scenario where interference management schemes are considered a de-facto operational prerequisite is encountered in deployments of 4G wireless access networks, such as the ones defined in the 3GPP LTE standard. In such wireless networks, apart from the standard cellular-like deployment of outdoor BSs, the use of low-power small cellular BSs has gained an increasing popularity in recent years. This is because the existing cellular network operation is facing great difficulties to deliver broadband services to indoor users, due to significant losses provoked by certain construction topologies. The rise of LTE-based femtocells (i.e., indoor BSs) that cover the needs of short-range residential gateways, largely addresses the indoors

topology losses, while their small size optimizes the spatial reuse of radio resources. Indeed, femtocells make feasible the increase of achievable rates per area-unit by reusing the same frequency band assigned to the primary transmission (i.e., between the macro BS and macro UEs). However, the highlighted benefits come at the expense of in-band interference. This is because the simultaneous use of the same operating RF band with equal signal bandwidth can frequently result in Co-Channel Interference (CCI), which in turn could either dramatically deteriorate the performance experienced by the neighbouring macro UEs, or even suspend the provided service. This occurs when the Carrier-to-Interference Ratio (CIR; average received modulated carrier power in relation to the average received CCI power), is below certain critical levels. Thus, better interference rejection capabilities have to be employed during the design of both infrastructure nodes and fixed or mobile equipment.
Interference is hence a major obstacle that can impair the potential gains of small cells, especially when they are deployed in the context of heterogeneous multi-cell networks. For this reason, it is a paramount requirement to apply an adaptive DL transmission among the femto BS and the femto UEs in order to guarantee that no interference is caused to the primary DL communication. This adaptive signal transmission is driven by a suitably selected interference management scheme. In recent years, numerous researchers have proposed techniques to reduce the interference improve the link-reliability and increase the capacity and performance in macrocell/femtocell scenarios [1]. Moreover, numerous Inter-Cell Interference Coordination (ICIC) schemes have been proposed to serve the operational needs of LTE-based femtocells [2]. These schemes include both interference avoidance techniques [3, 4] and interference mitigation schemes [5, 6].

II. 3GPP LTE PHY-layer

The mobile WiMAX and the 3GPP LTE standards (Rel. 9) [LTE, 2010] feature many similarities. Indicatively, as in the case of WiMAX the LTE PHY-layer is based on a scalable OFDMA architecture, with bandwidths ranging from 1.4 to 20 MHz, supporting various MIMO transmission schemes (i.e., Space-Frequency Block Code - SFDM, beamforming and SM). Two CP sizes are defined, where the largest one occupies one quarter of the OFDM symbol (i.e., denoted as extended CP). The 3GPP LTE supports both the TDD and the Frequency Division Duplex (FDD) operating modes. In the FDD mode the OFDM symbols are organized in groups of 12 consecutive subcarriers, known as Physical Resource Blocks (PRBs). The number of PRBs included in each OFDM symbol depends on the bandwidth size (i.e.,100 in the 20 MHz case). When the extended CP is utilized, each group of six OFDM symbols is named a slot. Furthermore, two slots form a subframe and each frame is composed by ten subframes. The resulting radio frame, shown in Figure 1, is 10 ms long.

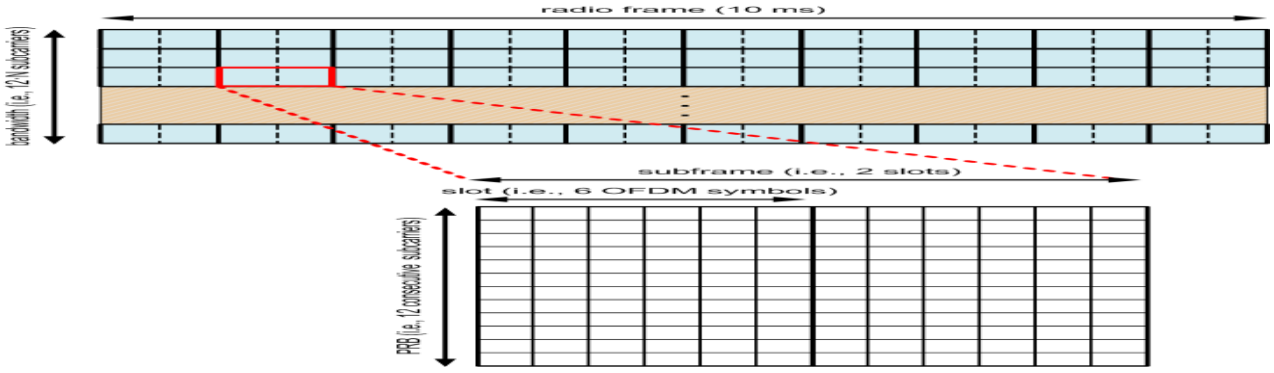


Figure 1: Basic time-frequency FDD LTE-frame structure.

As in the mobile WiMAX case, the pilot subcarriers, which in the LTE standard are denoted as Reference Signals (RSs), are distributed within the defined slots. The specific RS distribution of the previously presented FDD LTEframe can be observed in Figure 2. As it is shown, RSs are only transmitted in one of each three OFDM symbols. This feature is important, since the channel estimation needs to be calculated using groups of OFDM symbols (i.e., requiring an increased storage capacity). Additionally, four possible predefined I/Q values can be found for the pilot tones (i.e., $\pm 1/\sqrt{2} \pm 1/\sqrt{2}\, i$).Without entering into details, it must be noted that while the location of the RSs is exactly the same in all subframes, two different value-distributions are applied to each half of the frame (i.e., known RS-value sets are defined for each five-subframe set). Apart from the RSs, the LTE DL frames also include two additional sets of predefined-value subcarriers, namely the Primary Synchronization Signal (PSS) and the Secondary Synchronization Signal (SSS), which facilitate the cell iden -tification and synchronization of the UEs. The PSS can be found in the last OFDM symbol of both the first and sixth subframes, while the SSS is always located at the OFDM symbol preceding the one containing the PSS. In an FDD scheme an uninterrupted flow of data is received in the time domain, hence the known location and values of the PSS and SSS allows the identification of the precise subframe that is being received.

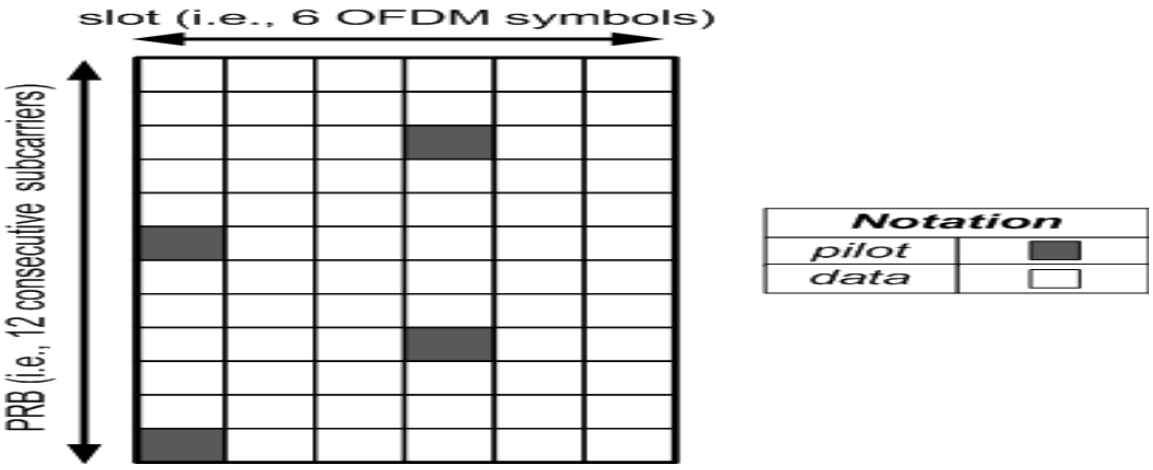


Figure 2: RS distribution utilized in the FDD LTE-frame.

III. Considered scenario and PHY-layer specifications

Designing and implementing an interference management scheme to operate in realistic conditions is a representative situation where the specifications of the underlying analog RF components, signal converters, together with the realization of the DSP algorithms using baseband signal processing boards is an important issue to take into account from the very early stages of development. In fact, the credible validation of this type of algorithms implies the use of a real-time testbed that comprises a series of heterogeneous equipment. Each of the underlying hardware components has an impact on the performance of the developed algorithms. Whereas essential, the computer-based modeling can only be considered as a first step towards the real-life implementation and performance validation of a complex system. The interference mitigation in LTE-based HetNets is a typical case where the real-life implementation of the PHY-layer using a dedicated real-time baseband processing solution, accounts for the low-level hardware specifications and limitations of the target platform (digital and analog), the signal impairments, the features of the propagation channel and other physical constraints; such factors and conditions are not

always considered or thoroughly emulated when modeling the same PHY-layer using a high-level computer-based simulation. For this reason, the development of such algorithms should naturally target a proof-of-concept implementation of the PHY-layer using close to real-life operating scenarios. Among a variety of pragmatic considerations, real-time PHY-layer implementations like the one that is presented in this chapter, take into account the translation of the floating point arithmetic of the initial high-level system model to a fixed-point one, the finite processing resources and capacity of the selected real-time baseband processing solution and the high impact on the overall development complexity

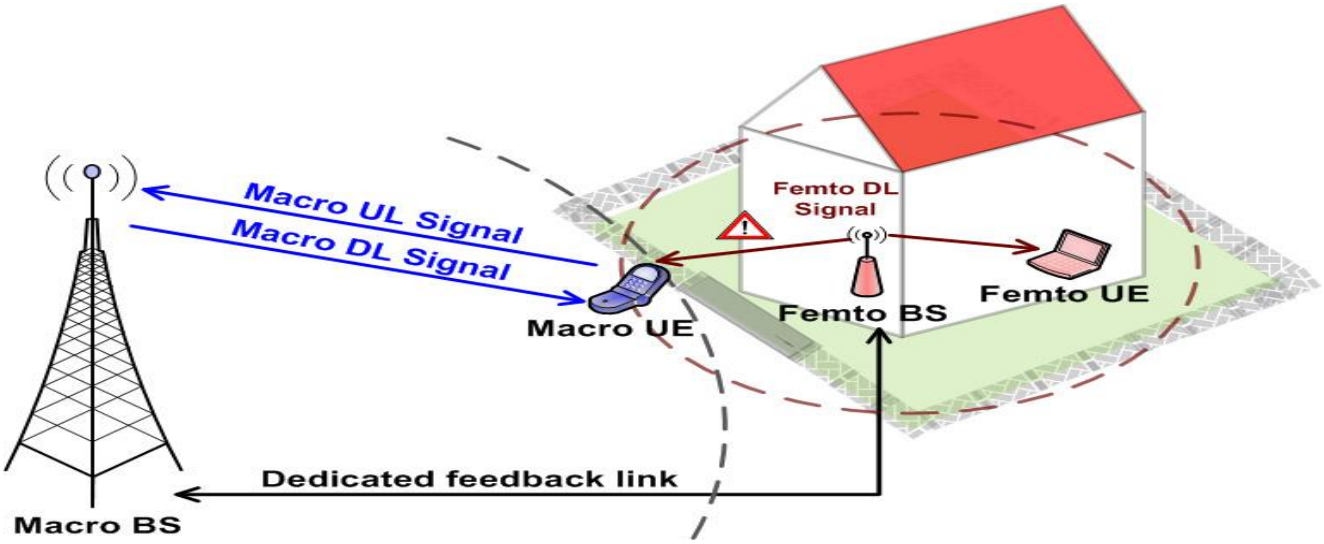


Figure 3: Considered LTE-based macrocell/femtocell frequency reuse scenario.

of the low-level control plane design (i.e., especially when it is required high run-time adaptively of the PHY-layer building blocks). When combining wide channel bandwidth (e.g., 20 MHz or more) and adaptive baseband algorithms whose performance or operability heavily depends on the instantaneous channel response at the mobile receivers, it is fair to claim that current computer-based simulations are struggling to cope with the required run-time processing load. Implementing the mentioned systems in specialized signal processing platforms resolves the performance and validation issues. Nevertheless, a wide and densely populated channel bandwidth brings additional considerations when implementing a real-time system at a chosen baseband signal processing platform (i.e., storage of large chunks of data, fast access of data, control plane with high complexity and interdependencies, bit-intensive signal processing at baseband). To illustrate the necessity of DL interference management strategies, the scenario depicted in Figure 3 has been considered, where the primary DL communication between a given macro BS and a macro UE is receiving interference from a secondary DL communication between a femto BS and a femto UE. The femto BS applies an opportunistic transmission at the same RF band and with the same bandwidth as the primary macro communication. For the sake of simplicity, the femto UL signal is not depicted in the figure. As it can be observed in Figure 3, the macro UE is located near the cell edge and near the femto BS, hence becoming a potential victim of in-band interference caused by the secondary transmission. If no interference management strategy is implemented and applied at this system, the quality of the signal received by the macro UE may significantly degrade, and thus negatively affect the QoS perceived by the end user (macro UE). To avoid this undesirable situation an interference mitigation technique for the femto BS is put in place, based on a self-organized PRB allocation scheme. More specifically, if the

macro UE detects interference in the DL signal, it notifies its associated BS (through a dedicated feedback link) which, in turn, requests the femto BS to adapt its transmission in order not to interfere the primary communication. The presented use case provides a baseline validation of this interference management scheme demonstrating the benefits in a practical and tangible way. Both case studies described in this thesis focus on point-to-point DL communications. In the case study presented herein, both the UL communication between the macro UE and the macro BS and the one between the macro BS and the femto BS are emulated. As in the first use case, only a subset of the PHY-layer features described in the LTE standard were implemented. Nevertheless, the considered DL OFDM frame is respecting the format described for the FDD operation mode in the LTE standard. It is important to underline that a high bandwidth of 20 MHz was selected, which as discussed earlier is influencing the amount of required processing resources (and thus depending on the target FPGA device, it may influence as well key design and implementation decisions). Table 1 summarizes the PHY-layer specifications. In more detail, the LTE-based frames were formatted in a suitable way to serve the proof-of-concept needs of the macrocell/femtocell interference-management mechanism, comprising periods where no data-transmission occurs. This implies that the UE knows a priori that no PRBs are allocated in given zones of the frame (i.e., non-active OFDM symbols). In the primary communication, all the PRBs in the active OFDM symbols are dedicated to the macro UE. The macro UE feedback defines which PRBs must be activated for the femto UE in the opportunistic femto transmission scheme. The RSs are included in all the OFDM symbols in the frame (i.e., active and non-active). The resulting quasi-quiet periods facilitate vital DSP operations implemented by the DFE of the receiver, such as the correction of the CFO or the AGC gain-modification. Figure 4 shows the utilized frame structure, where it can be observed that two different 5ms-frames are transmitted in the 10 ms period defined in the LTE standard.

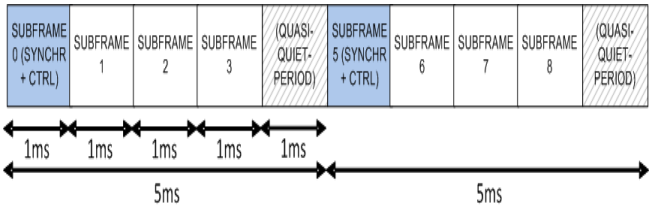


Figure 4: Specific frame format utilized in the LTE-based system.

Although the PSS and SSS structures are included in the transmitted LTEframe, a simpler synchronization method was employed based on the symbol repetition introduced in the DL signal by the CP. The pathloss model for suburban deployment of LTE femtocells, defined by the 3GPP [(3GPP), 2009], was adopted to define the range of acceptable Signalto-Interference Ratio (SIR) values. In order to achieve this, it was necessary to model the pathloss of the three DL signals. Hence this model included the DL communication between the macro BS and the macro UE, the equivalent femto DL communication and finally the interfering signal between the femto BS and the macro UE. It has to be noted that no interference was assumed for the femto DL communication due to the macro BS transmission. Therefore, in the proposed proof-of-concept, the SIR is defined as the ratio between the signal generated by the macro BS and the interfering signal. Apart from the pathloss model, other parameters such as the macro UE speed, the inter-site distance and the house size were also taken into account in order to finally define a SIR level between 12 and 20 dB for our considered testing scheme. Despite the fixed PHY-layer parameters and the simplified FDD transmission

scheme, the developed system is a complete real-time baseband prototype which accounts for real-life channel propagation and interference conditions.

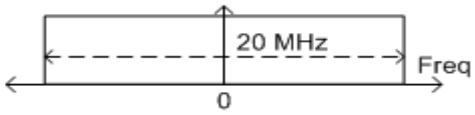
Table 1: Considered LTE PHY-layer specifications.

Parameter	**Value**
Wireless telecommunication standard	3GPP LTE (Rel. 9)
Antenna scheme: SISO	1x1
Channel bandwidth (MHz)	20
Cyclic prefix (samples)	512 (1/4 of the symbol)
Modulation type	QPSK
Duplex mode	FDD
Active subcarriers per OFDM symbol	1200
Null subcarriers per OFDM symbol	848
FFT size	2048
OFDM symbols per frame: total ||active	120 ||83
Closed-loop transmission scheme	Interference-aware
ADC sampling frequency (MHz)	PRB allocation
Baseband sampling frequency (MHz)	61.44
RF band (GHz)	30.72
IF (MHz)	2.6
Tested channel model	46.08
	ITU Ped. B (up to 3 km/h)

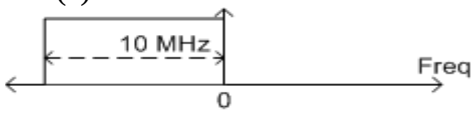
Interference management scheme

A novel distributed ICIC technique, known as Victim User Aware Soft Frequency Reuse in macrocell/femtocell HetNets [Shariat et al., 2012], was selected to realize the proof-of-concept interference management scheme. The main objective of this technique is to protect the macro UEs from the DL transmission of a neighbouring femto BS. In a frequency reuse scenario where both macro and femto communications utilize the same RF band, the available bandwidth is divided in various subbands. In

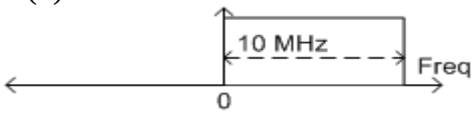
order to achieve dynamic interference mitigation, the instantaneous channel condition of the macro UE (victim) is exploited to adapt the femto transmission (i.e., to avoid interfering the primary communication). A basic objective is to deactivate the lowest number of required subbands in the secondary femto communication. Thus, the proposed technique aims at improving the throughput of the macro UE, while minimizing the impact on the performance of the femtocell. A downscaled version of the previously described interference management scheme was adopted, in order to reduce the implementation complexity without compromising the proof-of-concept goals; this featured a single macro BS/UE pair and one femto BS/UE pair. In this proof-of-concept case, the macro BS DL transmission uses the whole 20 MHz bandwidth, whereas the femto BS DL transmission uses two predefined 10 MHz bands. As it may be observed in Figure 5 these result in four different femto DL transmission-schemes (i.e., adaptive PRB allocation).



(a) Whole-band transmission



(b) The low 10 MHz band is used



(c) The high 10 MHz band is used

(d) The femto BS remains quiet

Figure 5: Predefined femto PRB allocation cases.

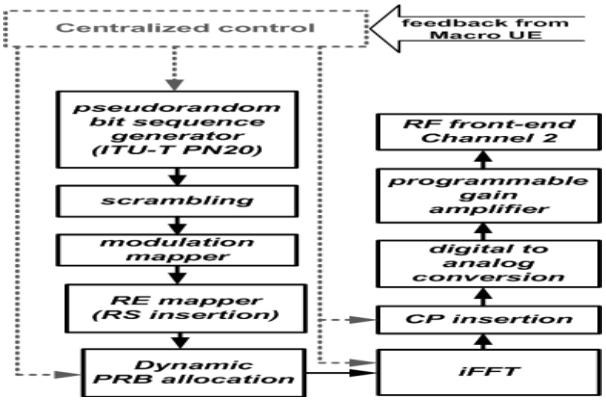
As previously mentioned, the macro BS and femto BS DL signals use the same RF band; hence, if both signals occupy the complete 20 MHz bandwidth and the mobile channel between the femto BS and the macro UE is not featuring deep fading in any of the defined 10 MHz bands, then the interference caused by the femto BS would prevent or severely impair the DL communication between the macro BS and the macro UE. For this reason, the macro UE requests at run-time a different femto BS transmission-scheme. In more details, the PRB allocation of the femto BS is dynamically adapted according to the performance requirements of the macro UE, which are subject to the instantaneous channel conditions. The starting point of the interference management scheme is encountered in the macro UE, which executes an interference-detection algorithm that determines if there is presence of interference or not. On top of that, the algorithm specifies the band(s) where interference is detected. Using that information, a feedback is generated defining which of the four femto BS transmission modes is going to be used. The interference management decision tries to guarantee the best femto DL communication. Hence, the no-transmission scheme is forced only when the interference is detected in the complete 20 MHz bandwidth. Finally, the femto UE is able to follow the adaptive PRB allocation.

Utilizing an incremental development

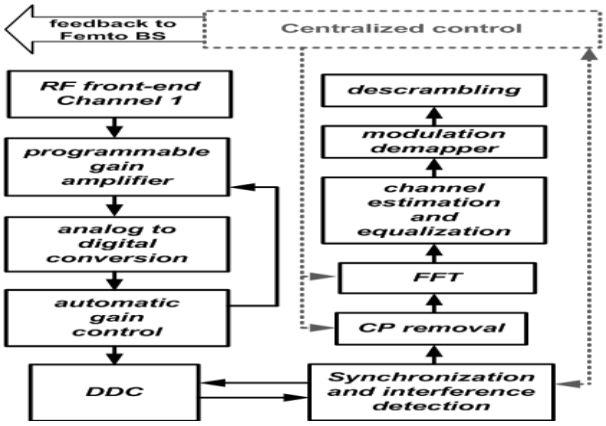
The interference-mitigation scheme presented in this chapter can be considered an evolution of the single-antenna system. Although the underlying wireless communication standard is different, part of the RTL design presented in the previous chapter has been reutilized. To start with, the model of the signal received at the macro UE features a great similarity.

$$c(t) = R\{x(t).e^{j2\pi(f_{IF}+\Delta f)}\} + R\{u(t).e^{j2\pi(f_{IF}+\Delta f_u)t}\} + A + B.\cos(2\pi(f_{IF} + \Delta f_u)t + \varphi) + w(t)) \quad (1)$$

where $x(t)$ represents the useful part of the received baseband signal, $u(t)$ is the interference, f_{IF} is the IF, Δf and Δf_u are the CFO for the desired and interfering signals respectively, A is the DC level introduced by the baseband board chassis, $B.\cos(2\pi(f_{IF} + \Delta f_u)t + \varphi)$represents the unwanted residual carrier, located at the center of the useful signal-spectrum (i.e., introduced by LO



(a) Femto BS



(b) Macro UE

Figure 6: General block-diagram of the implemented LTE-based PHY-layer.

coupling at the transmitter) and finally, $w(t)$ is the zero-mean white circularly symmetric Gaussian noise. The received baseband signals can be expressed as follows:

$$x(t) = \tilde{x}(t) * H(t),$$

$$u(t) = \tilde{u}(t) * Hu(t),$$

where $\tilde{x}(t)$ is the equivalent transmitted baseband signal, $\tilde{u}(t)$ represents the equivalent interfering baseband signal and $H(t)$ and $Hu(t)$ are the equivalent baseband representations of the corresponding channel responses for the desired and interfering signals, in respect to the center RF frequencies, f_{RF} +Δf and f_{RF} +Δf_u, of each of the two signals. The focus of this chapter is on the design of an extended DFE, which provides the core functionalities of the interference-mitigation scheme. The baseband processing stages of the femto BS and macro UE are shown in Figure 6. Taking advantage of the incremental development principles, the re-utilized building blocks are listed hereafter:
(i) Certain processing blocks have been directly reused (i.e., symbol mapping/ de-mapping, insertion and removal of the CP and FFT/IFFT). Similarly, the PRBS generator utilized at the macro BS is directly reused from the WiMAX system, whereas a variation of the same logic, based on the ITU PN20 specification [(ITU), 1996], has been selected for the femto BS.
(ii) The LTE-based system also takes advantage of the channel estimation processing architecture that was presented for the WiMAX receiver. For

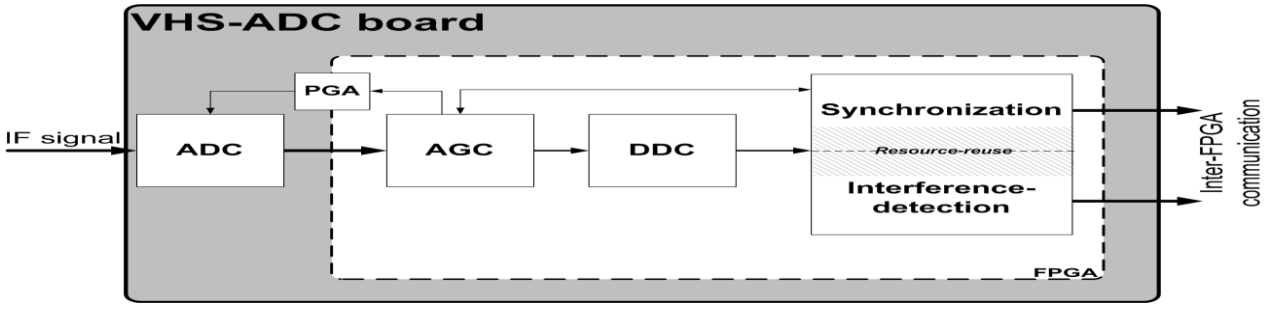


Figure 7: Extended DFE architecture of the macro UE.

instance, the speed-optimized pipelined DSP structure that calculates the quadratic interpolation was directly reused. At he same time the internal memory system and neighbouring pilot-set selection algorithmic had to be slightly modified considering that the channel estimation in LTE is performed for each group of three OFDM symbols (inWiMAX the channel was estimated using OFDM symbol pairs) and according to the defined RS distribution.
(iii) The core DFE functionality is an adapted version of the one presented in the first use case. The modifications are encountered in the AGC, which takes into account the longer frame format, and also in the DDC and synchronization processing stages, which were configured according to the
LTE system specifications (recall Table1). As already mentioned, the DFE of the macro UE was extended to provide the required interference management features, as it is detailed in the following section.

Operation of the extended DFE
The DFE plays a critical role in the correct operation of any real-life receiver and greatly influences the overall performance of the system. The role of the AGC and DDC is to exploit the full dynamic range of the received signal and provide the baseband signal respectively (i.e., sampled at 30.72 MHz as defined by the LTE standard); the synchronization on the other hand, locates the FFT window of each OFDM symbol, estimates the CFO (which is used to re-tune the DDS of the DDC) and controls the operation of the AGC. On top of these core DFE functionalities, the macro UE needs to detect in a timely manner any interference that might originate from the femto BS DL transmission, since its presence might prevent the decoding of the received signal. Thus, the functionality of the DFE has been extended to include

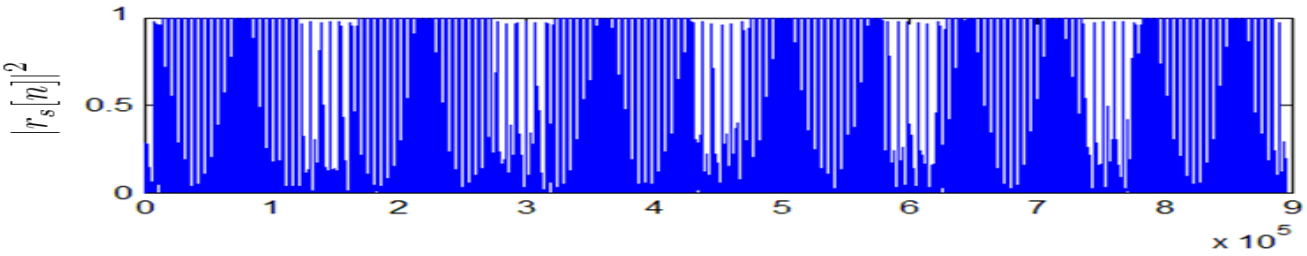
interference detection capabilities which were also complemented with feedback generation and signalling features. A high-level representation of the proposed interference-aware DFE is presented in Figure 7. Taking into account that this design has to be hosted in a single Virtex-4 LX160 FPGA device, it was required to employ a rigorous resource-reuse strategy at algorithmic level.

Interference-detection algorithm: design decisions for a resource-optimized RTL design

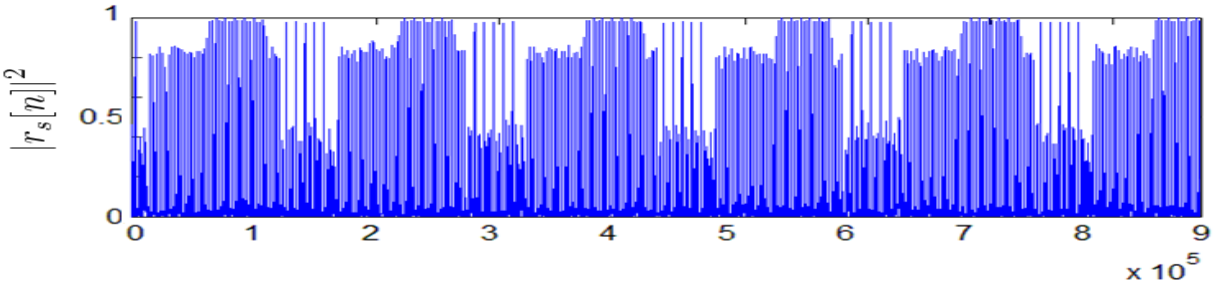
Taking into account the defined scenario, the proposed interference-mitigation scheme relies on a joint implementation of the synchronization and interference detection mechanisms. The symbol synchronization (i.e., location of the FFT window) was designed exploiting the self-similarity of the received OFDM symbols due to the presence of a CP at the beginning of each symbol. Likewise it was achieved a re-utilization of the synchronization technique .Moreover, it was avoided to implement the far more complex synchronization method that is based on the utilization of the SSS/PSS signals of the LTE-based DL frame (hence, saving useful FPGA resources). An algorithm optimization, favouring a minimization of the required computation resources, is applied to achieve an interference-aware synchronization technique. Specifically, as in the case of theWiMAX receiver, a cross-correlation is performed to detect the CP and locate the FFT window of the samples comprising each OFDM symbol. Furthermore, the values of the cross-correlation can be opportunistically reused to detect the presence of a non-negligible interference in the DL signal, relying on the fact that the degradation of the cross-correlation utilized to locate the CP is directly related to the SIR conditions at the receiver (i.e., the peak values of the correlation decrease in the presence of an interfering femto DL signal). When the interferer's CP is aligned in time with the CP of the received user data frames, the interference is denoted as synchronous, whereas when the CPs are not aligned, it is denoted as asynchronous. In the considered system, given the nature of the proposed interference-detection mechanism, it is assumed that the interferer is asynchronous. The calculation of the cross-correlation follows the same algorithmic rationale of the first use case, which was appropriately adapted to meet the specifications of the considered scenario. More specifically, given the impulse response of the considered ITU Pedestrian B channel model, the sliding window utilized in the main processing branch was resized to 2048+467 samples (i.e., 45 samples were discarded due to the effect of the mobile channel). The expression corresponding to the square of the correlation when the sliding window starts at the *n*th sample is given by:

$$|r_s[n]|^2 = \frac{\left|\sum_{l=0}^{466} s^*[n+l].s[n+l+2048]\right|^2}{\left(\sum_{l=0}^{466}|s[n+l]|^2\right).\left(\sum_{l=0}^{466}|s[n+l+2048]|^2\right)} \quad (2)$$

where $s[n]$ is the equivalent complex baseband signal at the output of the DDC, sampled at 30.72 MHz. A peak in $|r_s[n]|^2$, indicates the detection of the symbol and thus the sample where the CP starts. In a scenario without noise and without interference, the amplitude of the peaks of $|r_s[n]|^2$ is almost equal to one. Nevertheless, in the presence of noise and interference the cross-correlation profile is degraded and the amplitude of the peaks decreases, as it can be observed in Figure 8. The amount of degradation is directly related with the power of the received interference. Hence, the presence of interference can be detected by accurately defining a threshold value (i.e., a peak value below the defined threshold indicates the presence of interference). Figure 9 shows an overview of the baseband processing architecture that was designed towards this end.



(a) No interference is present



(b) SIR of 12 dB.

Figure 8: Degradation of the cross-correlation profile in the presence of interference.

The interference detection scheme is based on three signal processing branches. The main branch jointly implements the synchronization and the interference-detection mechanism, which scans the entire 20 MHz band to identify the presence of interference. The other two branches detect interference on two predefined 10 MHz subbands. These half-band interference detectors are built with the help of precise low-pass and high-pass complex filters (i.e., a complex-valued FIR stage is applied to the baseband signal produced by the DDC, in order to separate each defined 10 MHz band). Furthermore, a latency-compensation FIFO memory (dimensioned according to the latency of the digital filtering stage) ensures the time-alignment of the three interference-related DSP branches. The proposed interference detection algorithm tracks the effect of interference on the normalized CP correlation. For this reason it was necessary to define a threshold in this correlation; if the minimum correlation peak of a given data period is below this threshold, then interference is detected. In order to decide if the interference is present in the whole bandwidth, or in the upper or lower half of the band, Algorithm 1 is applied at each 5 ms-frame. The three processing branches are producing the inputs of the feedback generation block, which is reduced to a basic logic table, that provides a twobit feedback signal (i.e., 00 = no interference, 01 = interference in the low 10 MHz band, 10 = interference in the high 10 MHz band and 11 = whole-band interference). Finally, the architecture is completed by a centralized unit (found in the whole-band detection branch) which implements the control-plane of the proposed PHY-layer scheme.

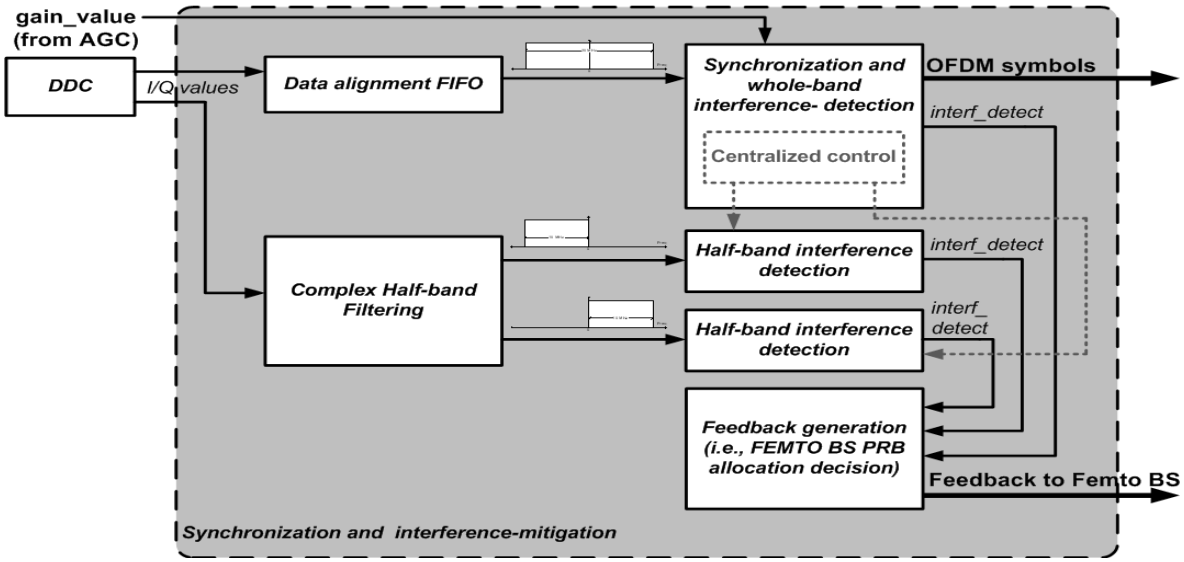


Figure 9: Joint synchronization and interference-detection design.

Algorithm 1

if wholeband_detection == 0 then
decision = no interference;
else
if low_10MHz_band_detection == 1 and high_10MHz_band_detection == 0 then
decision = interference detected in the low 10 MHz band;
else if low_10MHz_band_detection == 0 and high_10MHz_band_detection == 1
then
decision = interference detected in the high 10 MHz band;
else
decision = interference detected in the entire bandwidth;
end if
end if

IV Efficient RTL design of the complete communication scenario

While the proposed interference-management scheme might seem simple at algorithmic level, its realistic validation demands a complex digital realization that is heavily conditioned by the challenging PHY-layer features (i.e., large bandwidth, closed-loop communication, adaptive PRB allocation and interference mitigation capabilities) and the computationally intensive DSP functions. In fact, the joint synchronization and interference-detection/mitigation technique constitutes one of the most complex processing structures in the considered LTE-based system, since their building blocks result in a resource-hungry processing stage, featuring a number of complex FIR filters, a phase extraction function, one division and a number of multiplications among other arithmetic operations. Therefore, its real-time implementation requires a hardware-efficient RTL design which in fact is the main innovation presented in this chapter.
In the following subsections it is detailed the RTL design of the digital filtering stage, the joint synchronization and wholeband-detection technique and the centralized control unit.

Hardware-efficient implementation of a complex digital filtering stage

The MATLAB Filter Design and Analysis Tool (FDATool) was used to design the required low-pass and high-pass filters of the half-band interference-detection branches (recall Figure 9). The FDATool produces coefficients in a file-format tailored for the Xilinx FIR IP core. The FIR filter architecture accounts for a complex input signal; hence, the resulting filter coefficient-sets are also complex valued. Taking into account that the Xilinx FIR IP core only accepts real-valued coefficients, two instances are required in order to implement each complex filter (i.e., one for the real part, $h_i[n]$, and another for the imaginary part, $h_q[n]$). The filters have been designed satisfying a trade-off between its number of coefficients and the resulting out-of-band rejection. This trade-off also accounted for the available FPGA resources of the target platform. A suitable set of 51 18-bit complex coefficients was selected exhibiting an attenuation of 35 dB in the rejection band. The duplication of the FIR filters was an important design concern, since a combination of filters with such specifications consumes a large amount of FPGA-resources (DSP48 or generic slices depending on the underlying implementation particulars). For this reason resource sharing techniques

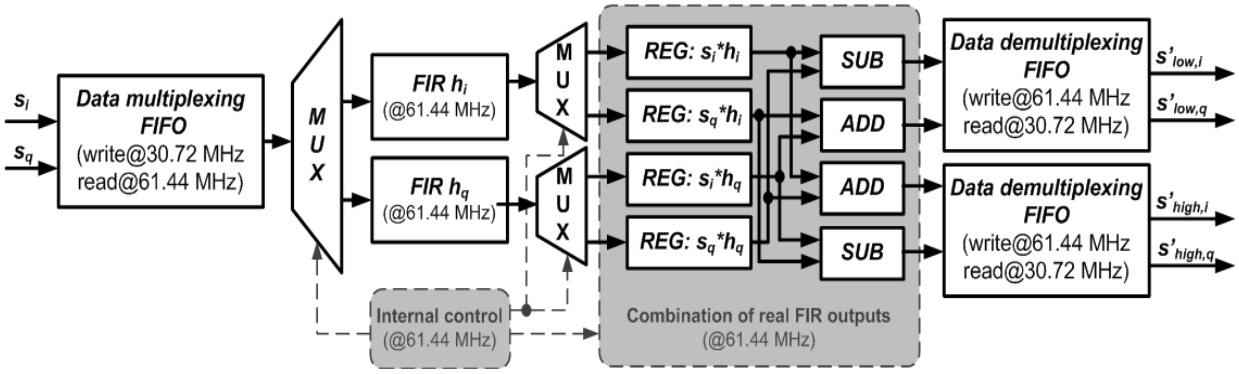


Figure 10: Proposed time-shared architecture for the complex FIR filters.

have been employed in order to tackle the limited capacity of the FPGA device in the target validation platform. An efficient way to reduce the implementation complexity was to design filters with symmetric response (featuring an even-symmetric coefficient set). Furthermore, the coefficients of the FIR filter that isolates the high 10 MHz band, *h*high[*n*], are the complex conjugate of its low 10 MHz band counterpart, $h_{\text{low}}[n]$, as indicated hereafter:

$$h_{\text{low}}[n] = h_i[n] + j \cdot h_q[n], \tag{3}$$

$$h_{\text{high}}[n] = h_i[n] - j \cdot h_q[n]. \tag{4}$$

The resulting RTL design is taking advantage of the previous characteristic as shown in Figure 10. The two complex filters were implemented using only two FIR filter instances by exploiting a resource-sharing architecture. A data-multiplexing technique is allowing this portion of the system to work at two-times the baseband frequency (i.e., 61.44 MHz). The FIR filters process real signals and feature two internal processing channels; this fact allows them to process concurrently two different input sample streams (i.e., the real and imaginary components of the produced I/Q data-stream are processed separately in an interleaved fashion). Whereas a new I/Q value is available each 32.55 ns, the two-channel FIR instances are requiring a new real-valued input each 16.28 ns. During the first half of each 32.55 ns time-slot, the real

component (i.e., first channel) of the incoming DDC output is delivered to the two filter instances. Similarly, its imaginary part (i.e., second channel) is introduced to the two filters during the second half of the 32.55 ns time-slot. In order to implement this solution, dedicated switches and FIFO memories with independent read and write clocks are utilized to provide a reliable cross-clock domain data communication. The produced filter-outputs are then demultiplexed to produce the complex filter outputs at the baseband frequency of, 30.72 MHz. In more detail, the real and imaginary operands of the incoming samples are processed sequentially in a custom pipelined architecture, as detailed hereafter:

(i) The incoming I and Q operands, $s_i[n]$ and $s_q[n]$, are stored at 30.72 MHz.
(ii) $s_i[n]$ is read at 61.44 MHz in the first processing channel of the filter.
(iii) The convolution of this operand with the real and imaginary operands of the filter coefficients is calculated (i.e., $s_i[n] * h_i[n]$ and $s_i[n] * h_q[n]$). In parallel $s_q[n]$ is read at 61.44 MHz in the second processing channel of the filter.
(iv) The outputs of the first channel of the filter are stored at 61.44 MHz. In parallel, the equivalent calculations are repeated for $sq[n]$ (i.e., $s_q[n] * h_i[n]$ and $s_q[n] * h_q[n]$).
(v) The outputs of the second channel of the filter are stored at 61.44 MHz.
(vi) The output-values of the complex filters, $s'_{\text{low}}[n] = s[n] * h_{\text{low}}[n]$ and $s'_{\text{high}}[n] = s[n] * h_{\text{high}}[n]$, are calculated as follows:

$$s'_{\text{low},i}[n] = s_i[n] * h_i[n] - s_q[n] * h_q[n] \quad (5)$$
$$s'_{\text{low},q}[n] = s_q[n] * h_i[n] + s_i[n] * h_q[n] \quad (6)$$
$$s'_{\text{high},i}[n] = s_i[n] * h_i[n] + s_q[n] * h_q[n] \quad (7)$$
$$s'_{\text{high},q}[n] = s_q[n] * h_i[n] - s_i[n] * h_q[n] \quad (8)$$

The detailed operations require two 16.28 ns time-slots (i.e., two-channel filters operating at 61.44 MHz).
(vi) The resulting output samples are stored at 61.44 MHz.
(vii) The filtered samples are read at 30.72 MHz and forwarded to the half-band interference detection components.

Joint design of the synchronization and the interference-detection

As it has been introduced previously, it is proposed a design favouring a minimization of the required computation resources, to achieve interference aware synchronization technique. The latter is based on the calculation of a cross-correlation to detect the CP heading each OFDM symbol. The reduced complexity RTL design presented for the WiMAX system was reutilized, in order to attain a minimized arithmetic-implementation cost here after:

$$|r_s[n]|^2 = \frac{|dn[n]|^2}{ds0[n] \cdot ds1[n]}, \quad (9)$$

where the elements in the numerator and denominator are calculated in a recursive way:

$$dn[n+1] = \begin{cases} dn[n] + s^*[n+467] \cdot s[n+2048+467] \\ \qquad \text{if } n \leq 467 \\ dn[n] - s^*[n] \cdot s[n+2048] \\ \qquad + s^*[n+467] \cdot s[n+2048+467] \\ \qquad \text{if } n > 467, \end{cases} \quad (10)$$

where $s[n]$ is the equivalent complex baseband signal at the output of the DDC, sampled at 30.72 MHz, and with $d_n[0] = 0$ ($d_s0[n]$, $d_s1[n]$ are calculated in a similar manner). With this optimization only four samples need to be introduced to the already calculated correlation, thus resulting in a much less DSP-block demanding FPGA realization. A reduced version is also implemented in each half-band interference-detection processing branch; taking into account the length of the impulse response of the complex filters, the sliding window is using 51 samples less.

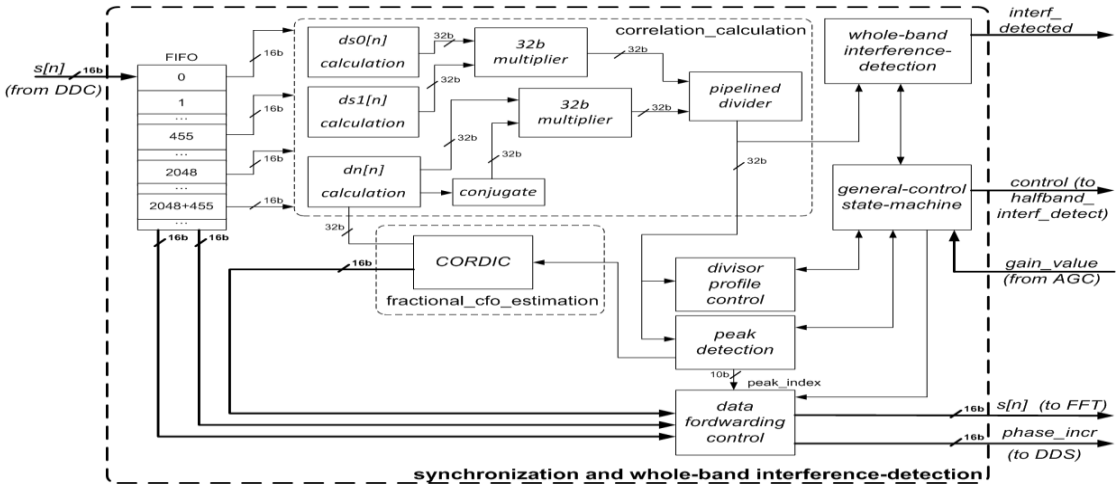


Figure 11: Detailed RTL design of the synchronization and wholeband interference-detection block.

The proposed RTL architecture for the joint synchronization and whole-band interference-detection technique extends the one utilized in the mobile WiMAX use case, as shown in Figure 11. It must be noted that the threshold-based peak detection mechanism has been adapted to the LTE signal format. Specifically, the transmission of the RSs produces peak-values during the quasi-quiet periods, when ideally a peak value in the correlation should indicate the location of the CP of an OFDM symbol containing user-data. Hence, to determine whether a correlation peak is located within a user-data period or not, the value of the divisor is used, since $d_s0[n] \cdot d_s1[n]$ is naturally higher during the user-data periods (as shown in Figure 12). For this reason, a control process keeps track of the peak-values of the divisor, accounting for the gainvariations applied by the AGC. Finally, it must be noted that the internally utilized registers are reset at the beginning of a newly detected 5ms-frame to avoid problems with the accumulated arithmetic-error due to the finite precision of the fixed-point representation. A dedicated state machine is in charge of implementing the whole-band interference detection, based on the values of the cross-correlation utilized for the symbol detection and the previously defined whole-band interference-detection threshold, Th_{whole} band. Further details are provided in the following section. The half-band interference-detection processing blocks are implementing a reduced version of the previously described architecture. This includes the calculation of the cross-correlation (using a sliding window of 416 samples), with the associated peak-detection and divisor profiling logic, and also a dedicated half-band interference-detection state machine.

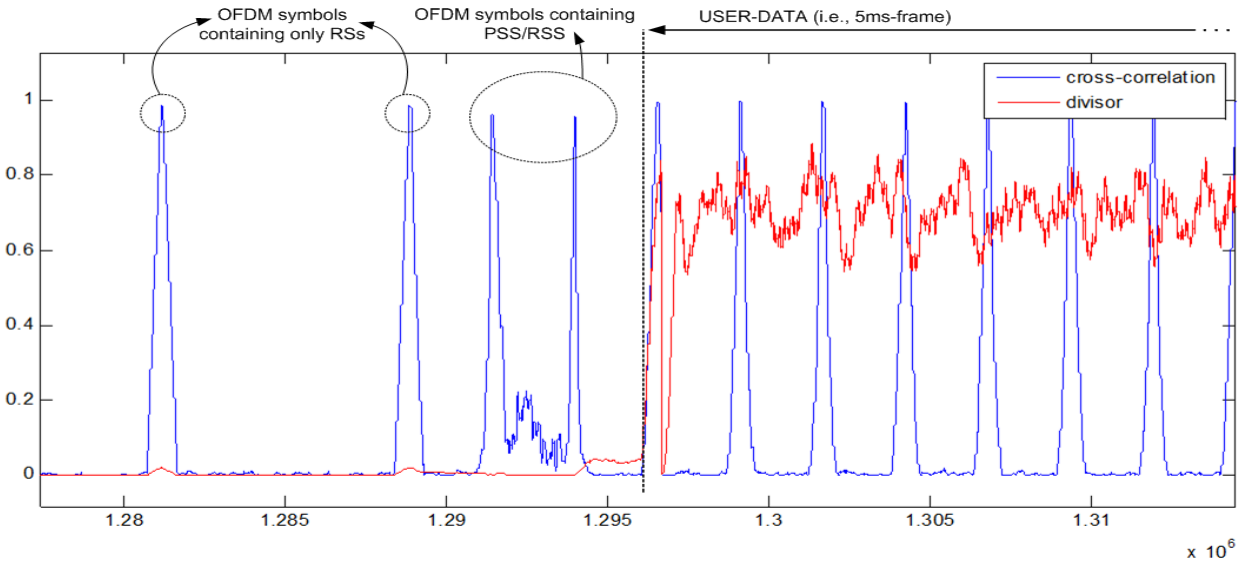


Figure 12: Cross-correlation and divisor values when a 5ms-frame is detected.

Centralized control unit

It is important to underline that the selected synchronization technique allows a low-complexity implementation of the interference-detection scheme. Nonetheless, the large number of concurrent DSP operations requires a carefully designed timing control of the diverse data-path stages. For this reason, a centralized controller was implemented to manage the synchronous operation of the above described sub-processes. This centralized control unit is also responsible for triggering the operation of the interference-detection DSP branches. In order to achieve resource-reuse, the control-plane of the DFE and its interference detection extension have been jointly addressed at design time, yielding an efficient FPGA implementation. This was achieved by utilizing a hierarchical structure of dedicated state machines. Figure 13 details the underlying state machine implementing the core functionalities of the centralized control unit of the macro UE. This unit tracks the symbol detection process, based on the values of the calculated cross-correlation, taking into account as well the values of its divisor. Likewise, it is detected the CP of the OFDM symbol including the PSS/SSS symbols of each 5ms-frame (i.e., FFT-window location). The symbol detection is then triggering both the operation of the interference-detection sub-blocks and the forwarding of data to the remaining baseband processing stages of the receiver. For the sake of clarity, the figure is not including the management of the AGC gain-variations (i.e., critically affecting the utilized divisor-threshold value). Similarly, the FFT/CP control processes, which are also activated with the symbol detection logic, have not been included. In Figure 13 it can also be observed the dedicated state machine used to control the whole-band interference-detection logic. Basically, if a single peakvalue within a 5ms-frame is below the defined threshold, then it will be indicated that interference has been detected in the main branch (recall Algorithm 1). The dedicated half-band interference-detection state machines present a similar structure and are managed by the centralized controller in an equivalent way.

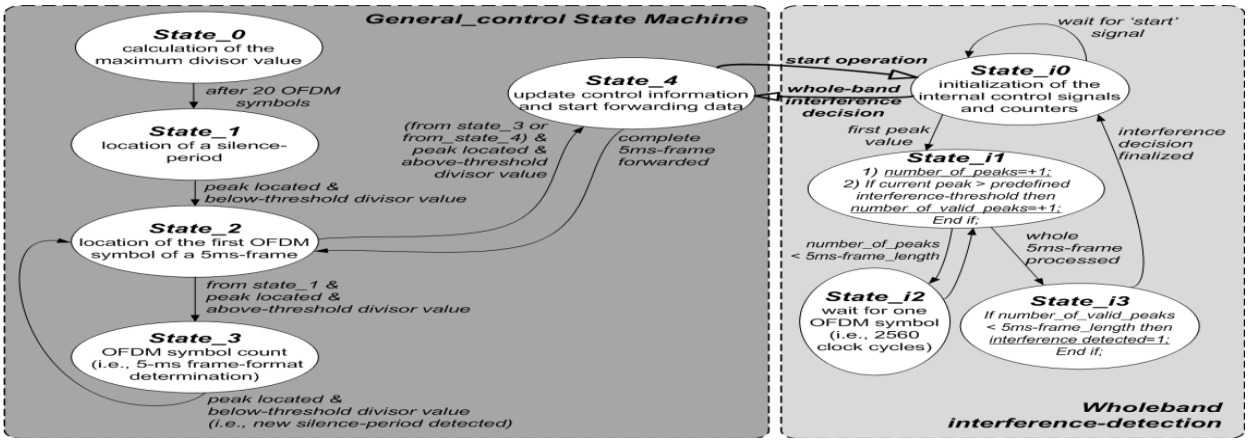


Figure 13: Indicative diagram of the designed control state machines.

V. Experimental results

As it was described before, the channel emulator was configured to provide a channel response between the macro BS and the macro UE according to the ITU Pedestrian B model. Furthermore, different interference scenarios have also been tested for both static and low-mobility conditions. A number of ChipScope FPGA-monitoring cores, embedded within the baseband design, have been used to get an insight of the interference-detection operation. Figure 14 is a screen capture of the Chipscope software which shows the evolution of the cross-correlation values in a scenario where interference is forced in the low 10 MHz band, with a SIR of 12 dB, while applying a static Pedestrian B channel model for the macro DL communication. As it can be observed, the correlation peaks are below the defined interference-detection thresholds, hence indicating that the DL signal of the macro UE is being interfered by the femto communication. During the experimental verification of the system it has been also utilized a real-time digital oscilloscope to inspect the generated RF signals (both at time and frequency domain). Figure 15 provides an indicative screen capture extracted from the mentioned instrument that demonstrates how the PRBs of the femto DL signal are adapted in real-time, when interference is detected (i.e.,as already described before, the transmitter is notified about the occurrence of this event through the feedback mechanism). The monitoring of the channel and interference effects was also facilitated by using a RF spectrum analyzer, as it is shown in the respective screen capture in Figure16; more specifically, the blue line represents the RF spectrum of the macro DL signal under ideal signal propagation conditions, the black line represents the same signal after a mobile channel (i.e., 3 km/h) has been applied and, finally, the green line shows the degraded spectrum in the presence of interference in the low 10 MHz band under mobile channel conditions.

In order to facilitate the experimental analysis of the proposed scheme, two transmission-modes were defined for the femto BS; one is based on the received feedback by the macro UE (i.e., applying adaptive PRB allocation) and the other forces a whole-band transmission (i.e., the feedback is ignored). Hence, during the experimental validation, the femto DL signal was generated by one of the two transmission-modes in fixed-length time-periods (i.e., this time-period could be modified on-the-fly through a user-controlled programmable register). Considering the need to evaluate the proposed test scenario under mobile channel conditions, and in order to avoid an extensive measurement campaign (such as the one featured in the mobile WiMAX system), it was decided to include additional logic in the macro UE to calculate the instantaneous BER (in a per frame basis); in order to achieve this, the PRBS generator of the macro BS was replicated in the receiver and its output was

compared with the de-mapper one. This real-time calculation of the BER metric avoids the tedious and lengthy data-capturing and post-processing; it also provided a great instrument to test, debug and validate the proposed interference-management scheme at run-time (i.e., by utilizing the ChipScope Pro software tool to visualize it).

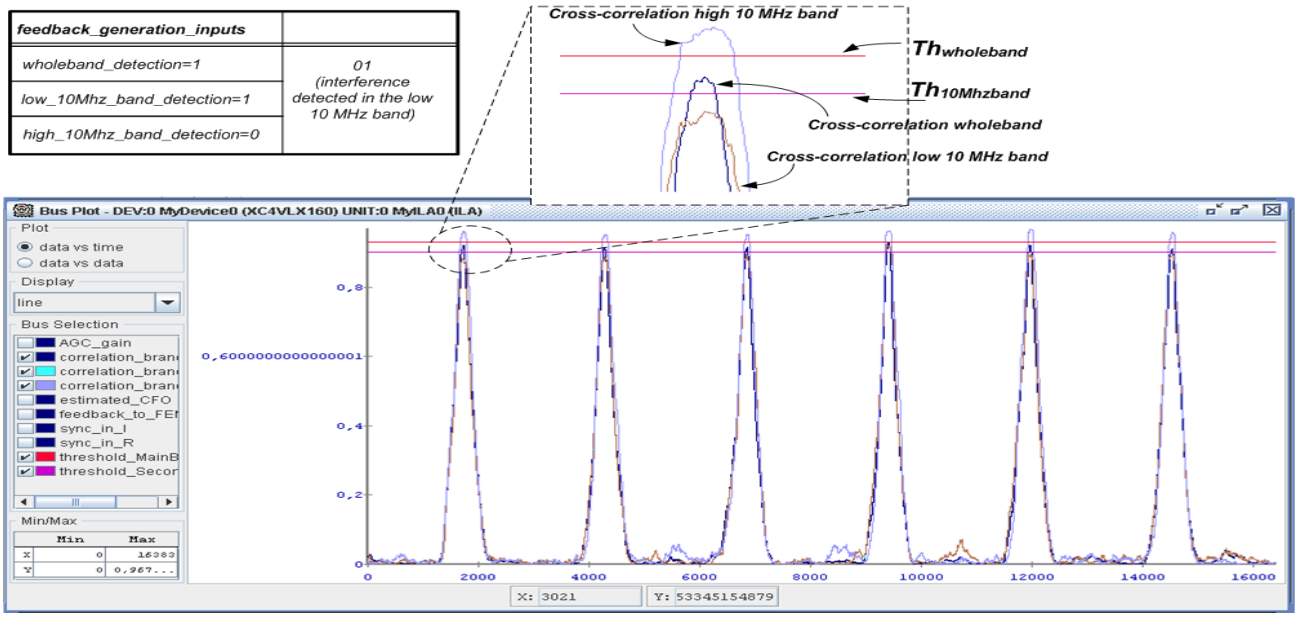
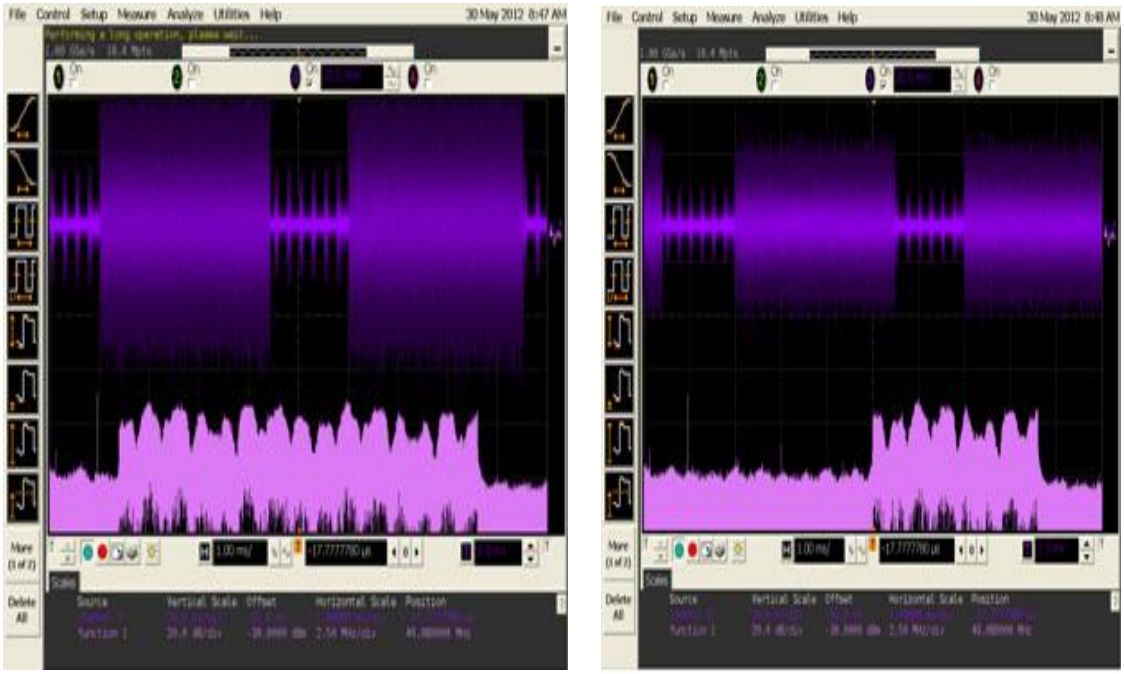


Figure 14: Cross-correlation versus the defined interference-detection thresholds for the 3 correlation chains at the macro UE.



(a) Whole-band transmission. (b) The high 10 MHz band is used.

Figure 15: Oscilloscope capture of the interference-aware femto DL signal.

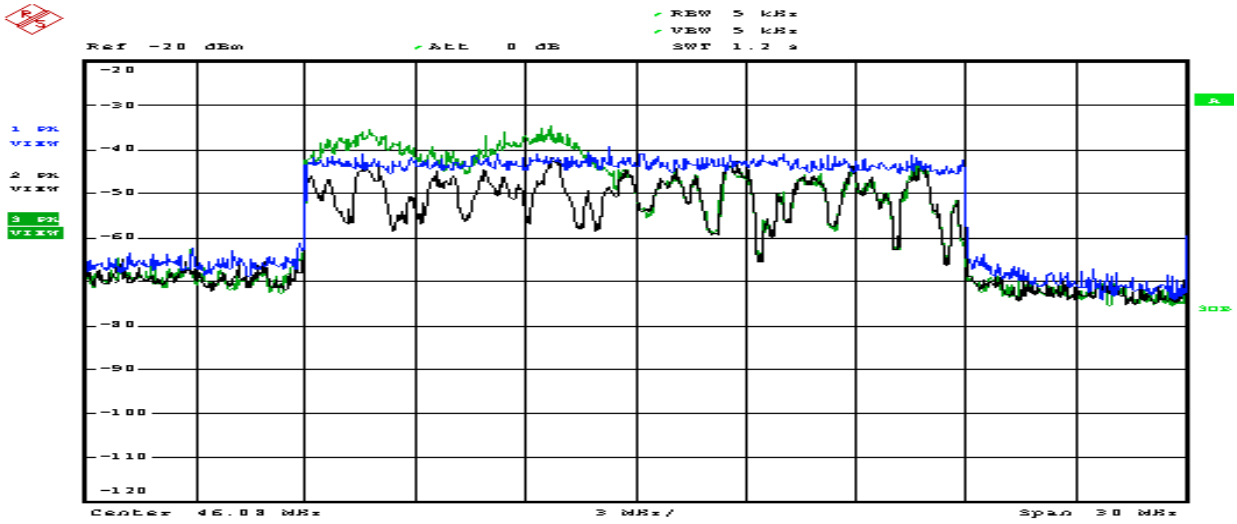


Figure 16: Visualization of the impairments introduced to the macro DL signal by both the mobile channel and the interference signal.

Figure 17 shows a representative Chipscope screen capture of the observed BER at the macro UE under the same interference conditions described before, for a lowmobility (i.e., 0.2 km/h) realization of the considered Pedestrian B channel model. The figure covers a period of 40 seconds (i.e., 8000 5 ms-frames). It has to be noted that the transmission-mode of the femto BS changes each 5 seconds. Moreover, it can be observed how the KPI is fulfilled during the periods where the PRB allocation of the femto DL signal is adapted according to the received macro UE feedback. Similarly, in 6.19it is repeated the experiment for a static channel realization, where a SIR of 10 dB is applied considering an interference on the whole 20 MHz band. Moreover, the evolution of the observed BER level for different SIR values (i.e., from 10 to 14 dB), in static channel conditions is provided by Figures 19a, 19b and 19c, where the considered interference is taking place in the upper 10 MHz band. Finally, a mobile channel (i.e., 3 km/h) and a SIR of 14 dB is applied to the same scenario, as it can be observed in Figure 19d.

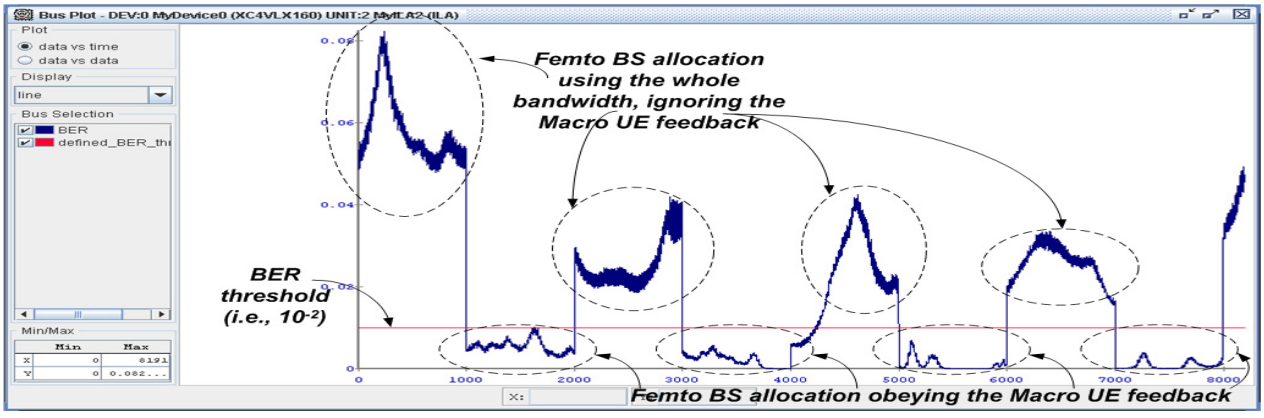
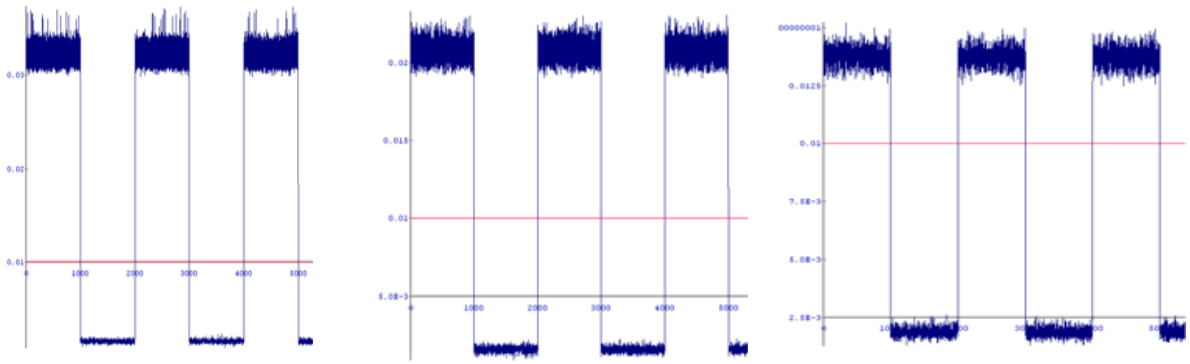


Figure 18: ChipScope screen capture depicting the macro UE BER under low mobility conditions and a SIR of 12 dB.



(a) SIR of 10 dB. (b) SIR of 12 dB. (c) SIR of 14 dB.

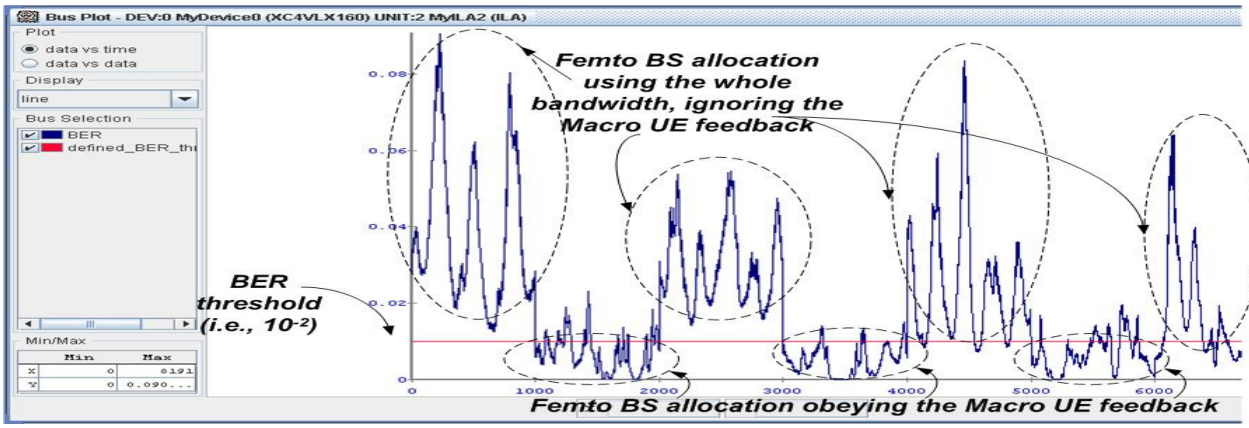


Figure 19: ChipScope screen capture depicting the macro UE BER for different SIR values and mobility conditions.

VI. Conclusion

The goal of these solutions was to maximize the parallelization and resource re-utilization of a number of DSP algorithms that form part of certain PHY-layer building blocks, in order to enable the efficient baseband design of modern wireless communication systems. Finally, some possible future work lines are proposed to extend the reach of the presented research.

In more details, the incremental development of a 2x2 MIMO closed-loop PHY-layer scheme, based on the mobile WiMAX wireless communication standard, provided the first use case of the proposed development methodology. Moreover, a second use case is provided by implementing an LTE-based macrocell/femtocell interference-mitigation scheme. This second use case was built upon an incremental design and IP re-utilization development strategy that took advantage of the outcome of the first use case. An important feature of the proposed RTL design techniques is that they are not confined to the implementation of wireless communication systems, but can be extrapolated to other use cases where bit-intensive DSP needs to be employed. Finally, it must be underlined how the presented use cases provide proof-ofconcept of advanced PHY-layer techniques which are meant to conform a vital part of the baseband of future wireless communication systems (e.g., multiantenna communications, adaptation of the DSP in response to the perceived channel conditions or interference-mitigation in a heterogeneous wireless accesstechnology scenario).

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Author Profile

Mr. A.M.Bharath Kumar Working as Assistant Professor in Department of Electronics and communication Engineering in *chaitanya Institute of Technology and Science, Markapur,Prakasam(Dist),Ap,India* .He recived M.Tech from SRM University in chennai . Now he persuing phd in hindustan universty in chennai.He has published many international journals. His current research interests are wireless communications,digital communications and channel estimation.