# Study the Analysis of Low power and High speed CMOS Logic Circuits in 90nm Technology

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## Abstract

This paper describes the parameter and characteristic analysis of Low power and High speed CMOS Logic Circuits in 90nm Technology. The proposed CMOS logic circuits consists only logic gates. CMOS circuit is fabricated in 0.12µm and 90nm CMOS technology. The supply voltage is 1.20V. The temperature was 27ºC. We observed Inverter (NOT gate) properties - MOS, Capacitance, Resistance, Inductance and Clock. These layouts can store in the form of semi-custom library to make full-custom SoC designs.

**Key words:** Low power, High speed, CMOS, Inverter and 90nm technology.

## 1. Introduction

The Semiconductor wafer is typically a slice of monocrystaline silicon about 0.2mm thick and perhaps 8 to 15cm in diameter. The wafer is divided checkerboard fashion in to 1000 or so rectangular areas. Each area will become a single chip. Each chip consist a digital circuits, for example, an inverter or an AND gate. An individual digital circuit may have only a few components, but some circuits have a few hundred components.

The need for low power design is a major issue in high performance digital systems, such as microprocessors, digital signal processors (DSPs) and other applications. The common traits of high performance ships are the high integration density and the high clock frequency. Several high performance microprocessor chips designed in the early 1990s operated at clock frequencies in the range of 100 to 300GHz, and their typical power consumption was between 20 and 50W. Modern microprocessors are running at clock frequencies above 1GHz with 100W power dissipation. [1]

In this paper we proposed, how SoC layout process for static combinational logic circuits in 90nm technology, for this purpose we developed a simple logic and combinational circuit like Inverter (NOT) layout by using CMOS logic circuits. And we studied its low power and high speed parametric analysis.

## 2. The 90nm Family and Benefits

The 90nm logic family includes general purpose (G), low power (LP), and high performance (GT) process options in 90nm and general purpose (GC) for digital

consumer applications in an 80nm process. The 80GC is a 90 percent linear shrink process from 90G. Each process supports multiple Vt options, including low, standard, and high, for improving power, speed, or leakage tradeoffs. Operating voltage is 1.0 – 1.2V; the I/O voltages range from 1.8 to 3.3 volts. [2]

The 90nm process provides numerous advantages over other technologies. It doubles gate density and boosts speed by 35 percent, a 60 percent improvement in active power savings, and a 20 percent intercontact RC improvement. The 90nm process is a full-fledged SoC plat form that provides both CMOS logic and Mixed-Signal/RF families. Embedded memory options include 6T SRAM, Electrical Fuse, One-Time Programmable (OTP), multitime programmable (MTP), Embedded Flash, and Embedded DRAM. The technology evolution and forecast up to 2011 is shown in table-1.

| Technology node | 180nm | 130nm | 90nm | 65nm | 45nm | 32nm | 22nm |
|---|---|---|---|---|---|---|---|
| First production | 1999 | 2001 | 2003 | 2005 | 2007 | 2009 | 2011 |
| Gate length | 130nm | 70nm | 50nm | 35nm | 25nm | 17nm | 12nm |
| Gate material | Poly $SiO_2$ | Poly $SiO_2$ | Poly $SiO_2$ | Poly SiON | Metal High K | Metal High K | Metal High K |
| Gate atoms | 10 | 8 | 5 | 5 | 5-10 | 5-10 | 5-10 |
| K gates/$mm^2$ | 100 | 200 | 350 | 500 | 900 | 1500 | ? |
| Memory point ($\mu^2$) | 4.5 | 2.4 | 1.3 | 0.6 | 0.3 | 0.15 | 0.08 |

Table-1 Technology evolution and forecast up to 2011

## 3. Static and Combinational CMOS design

A static CMOS gate is a combination of two networks, called the pull-up network (PUN) and the pull-down network (PDN). The PUN consists only of PMOS transistors and provides a conditional connection to $V_{DD}$. The PDN potentially connects the output to Vss and contains only NMOS device. The PUN and PDN networks should be designed so that, whether the value of the inputs, one and only one of the networks is conducting in steady state. [3] In this way, a path always exists between **$V_{DD}$** and **F** for an out put ("One"), or alternatively, between **Vss** and **F** for a low output ("Zero"). This is equivalent to stating that the output node is always a low-impedance node in steady state. Fig.1 shows the arrangement of this CMOS logic.

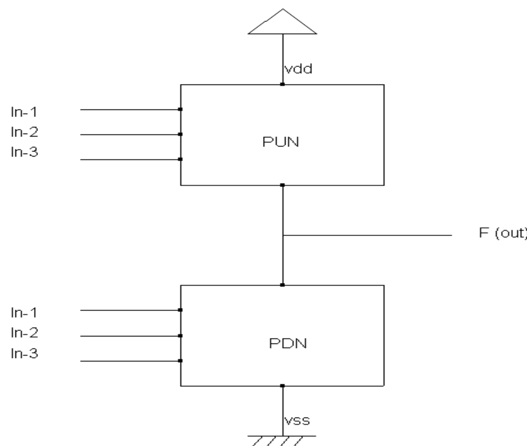


Fig.1: Complementary logic gate as a combination of a PUN and a PDN

A combinational system is a digital system in which the value of the output at any instant depends only on the value of the input at that same instant and not on previous values. Combinational systems are specified at two levels, high-level and binary-level. In a high-level specification, the system is described by a function on finite sets and represented by tables or expressions. In a binary-level specification all variables are binary; each variable has only two values, denoted by ‘0’ and ‘1’. [4]

## 4. Layout Layer representation in CMOS technology

The layer concept translates the intractable set of masks currently used in CMOS into a simple set of conceptual layout level that are easier to visualize by the circuit designer. From a designer’s view point, all CMOS designs are based on the following entities:

Substrates and/or wells, being P-type (for NMOS device) and N-type (for PMOS device).Diffusion regions (n+ and p+) defining the areas where transistors can be formed. These regions are often called the active areas. Diffusions of an inverse type are needed to implement contacts to the wells or to the substrate. These are called selected regions. One or more polysilicon layers, which are used to form the gate electrodes of the transistors (but serve as intercontact layers as well). One or more metal interconnect layers (typically **Al). ** Contact layers to provide interlayer connections. [5, 6]

A layout consists of a combination of polygons, each of which is attached to a certain layer. The functionality of the circuit is determined by the choice of the layers, as well as the interplay between objects on different layers. [7] In this present CMOS circuit fabrication we used poly and metal. The Poly width is 2 lambda, spacing is 3 lambda, surface capacitance is 400.00af/$\mu m^2$ and resistance is 4.00/sq ohm. The metal width is 3 lambda, spacing is 4 lambda, surface capacitance is 200.00af/$\mu m^2$ and resistance is 0.05/sq ohm. The Diff-n width is 4 lambda, spacing is 4 lambda, surface capacitance is 350.00af/$\mu m^2$ and resistance is 25.00/sq ohm. The Diff-p width is 4 lambda, spacing is 4 lambda, surface capacitance is 300.00af/$\mu m^2$ and resistance is 30.00/sq ohm. The Contact width is 2 lambda, spacing is 4 lambda, and resistance is 20.00/sq ohm.

## 5. MOS device Characteristics in 90nm Technology

## N-channel:

A Cross-section of the N-channel and P-channel MOS devices is given in figure-1. The NMOS gate is capped with a specific silicon nitride layer that induces lateral tensile channel strain for improved electron mobility. [8, 9] The I/V device characteristics of the low-leakage and high-speed NMOS devices listed in table-2 are obtained using the MOS model BSIM4.

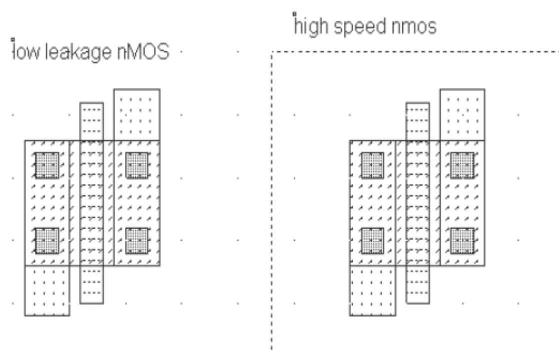


Fig. 2 Cross-section of the N-channel and P-channel MOS

| Parameter | NMOS Low leakage | NMOS High speed |
|---|---|---|
| Drawn length | 0.1µm | 0.1µm |
| Effective length | 60 nm | 50 nm |
| Width | 0.5 µm | 0.5 µm |
| Threshold voltage | 0.28 | 0.25 |
| Ion (Vdd = 1.2V) | 0.63 mA | 0.74 mA |
| Ioff | 30 nA | 300 nA |

Table-2: NMOS Parameters

## P-channel:

The PMOS drive current in this 90nm technology is as high as 700µA/µm for the low-leakage MOS and up to 800µA/µm for the high-speed MOS. These values are particularly high, as the target applications for this technology at Intel are high-speed digital circuits such as microprocessors. The leakage current is around 40nA/µm for the low-leakage MOS and near 300nA/µm for the high-speed device. The cross-section of the PMOS device reveals a SiGe material that induces compressive strain to obtain unmatched current capabilities near 1mA/µm. The I/V device characteristics of the low-leakage and high-speed PMOS devices listed in table-3 are obtained using the MOS model BSIM4.

| Parameter | PMOS Low leakage | PMOS High speed |
|---|---|---|
| Drawn length | 0.1µm | 0.1µm |
| Effective length | 60 nm | 50 nm |
| Width | 0.5 µm | 0.5 µm |
| Ion (Vdd = 1.2V) | 0.35 mA | 0.39 mA |
| Ioff | 21 nA | 135 nA |

Table-3: PMOS Parameters

## 6. CMOS Inverter (NOT) Gate Functionality

Fig.3 shows a simple CMOS inverter (NOT gate), **F = not A.** The PUN consists of one PMOS transistor, provides a connection from **Vdd (‘1’)**. The PDN, which consists of one NMOS transistor, provides a connection to **Vss (‘0’)**. This means that **F** is **‘1’** if **A=’0’**, and **F** is **‘0’**if **A=‘1’**, which is equivalent to **F= (not A).** It can be easily verified that the output **F** is always connected to either **VDD** or **Vss**, but never to both. Fig.3 (a) shows the logic gate symbol of inverter (NOT), Fig.3 (b) shows the CMOS NOT. Fig.4 shows the Inverter (NOT) functionality wave form.

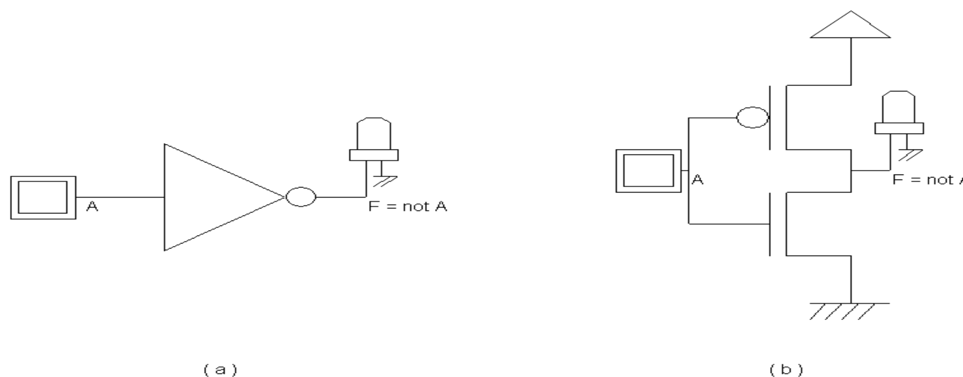


Fig.3 (a) logic gate symbol and (b) CMOS Inverter (NOT gate)

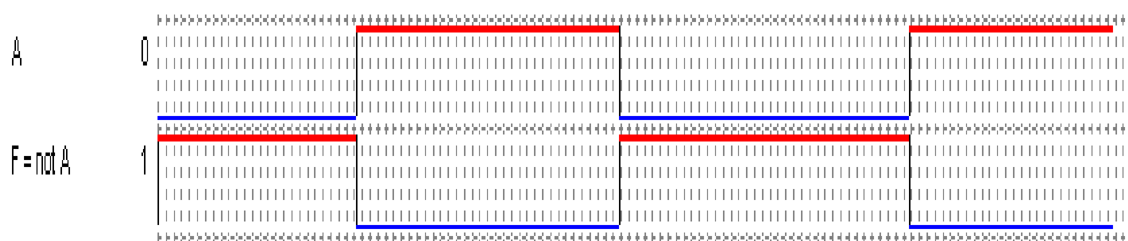


Fig.4 Inverter (NOT gate) functionality wave forms

## 7. Low power and High speed parametric verification of Inverter layout

The integrated circuit technology is one of the most important fields of the electronics since it minimizes the area of the circuit, parasitic effects and the cost. The increasing prominence of portable systems and the need to limit power consumption in very high density VLSI chips have led to rapid and innovative developments in low-power design the recent years. [10]

Here we studied and analysis the inverter (NOT gate) for low power and high speed performances. The inverter layout was fabricated in 90nm technology by using section 4 and 5 design rules. Fig.5 (a) shows the Low leakage and Fig.5 (b) shows the High speed layouts. The high speed MOS layout is capped with a specific silicon nitride layer that induces lateral tensile channel strain for improved electron mobility. Fig.6 shows the timing wave forms of the fabricated layouts. The width is 12.0µm (24 lambda), Height is 28.5µm (57 lambda) and Surf is 342.0µm2 (0.0 mm2) for low leakage layout. The Width is 13.0µm (26 lambda), Height is 36.5µm (73 lambda) and Surf is 474.5µm2 (0.0 mm2) for high speed layout. The temperature was maintained at 27ºC.

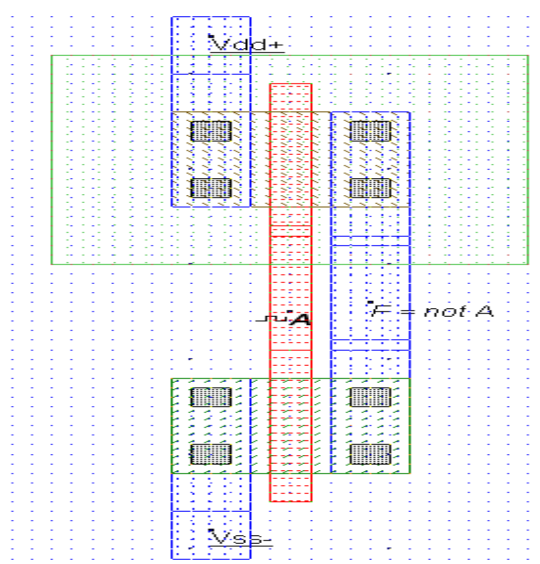


Fig.5: (a) Low leakage and (b) High speed Inverter (NOT gate) layouts in 90nm Technology

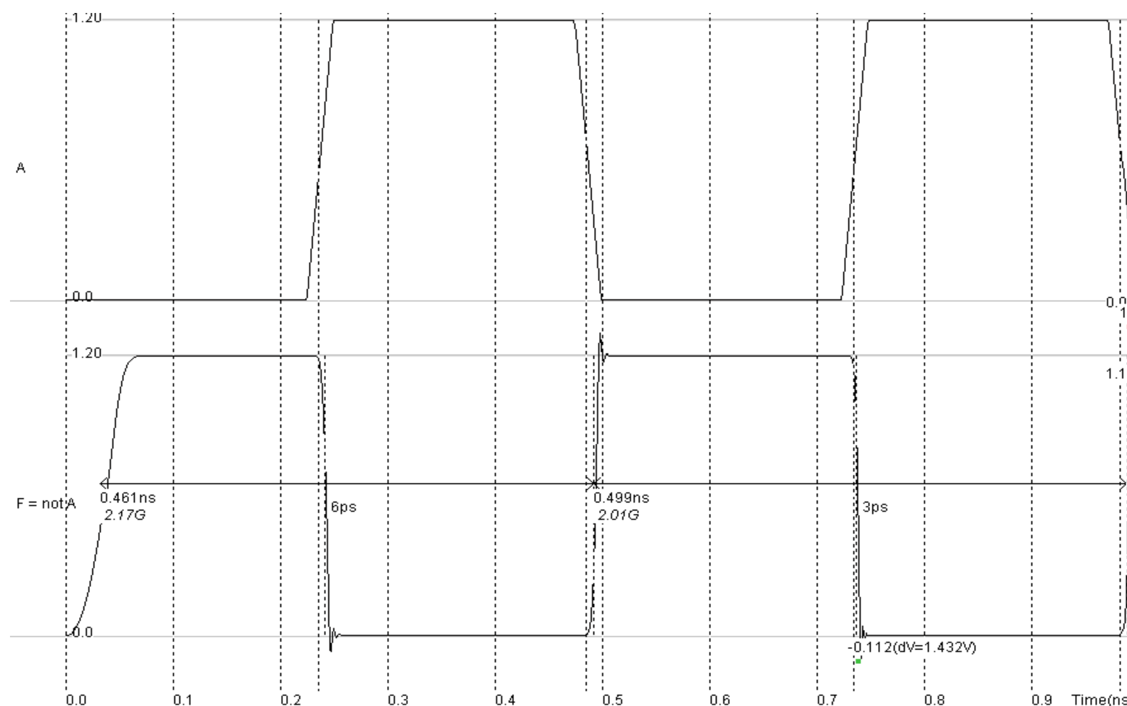


Fig.6: Inverter operation wave forms

To fabricate this inverter in the 90nm technology we defined the MOS parameters as shown in the table-4. The width, length, Imax is defined in µm and lambda design rule technology. The clock parameters – high level, low level, time low, rise time, time high and fall time are defined in table-5. Table-6 shows the node parasitic properties of low leakage Inverter Layout and table-7 shows the node parasitic properties of high speed inverter layout. Here we observed mainly capacitance, resistance, inductance and channel at the nodes of the layout circuit at nodes A, F=not A, Vdd and Vss.

| MOS Parameter | µm | Lambda |
|---|---|---|
| Width (W) | 0.6 | 10 |
| Length (L) | 0.12 | 2 |
| Imax (NMOS) | 0.635 mA | - |
| Imax (PMOS) | 0.390 mA | - |

Table-4: MOS parameters for Inverter Layout

| Parameter | Value |
|---|---|
| High level (V) | 1.20 |
| Low level (V) | 0.00 |
| Time low (tl) | 0.225 ns |
| Rise time (tr) | 0.225 ns |
| Time high (fh) | 0.225 ns |
| Fall time (tf) | 0.025 ns |

Table-5: Clock parameters

| Node | Capacitance (fF) | Resistance (Ohm) | Inductance (nH) | Channel (L) |
|---|---|---|---|---|
| A | 1.75 | 88 | 0.00 | 4 |
| F = not A | 0.41 | 190 | 0.00 | 4 |
| $V_{dd}$ | 0.20 | 100 | 0.00 | 2 |
| $V_{ss}$ | 0.21 | 90 | 0.00 | 2 |

Table-6: Node parasitic properties of low leakage Inverter Layout

| Node | Capacitance (fF) | Resistance (Ohm) | Inductance (nH) | Channel (L) |
|---|---|---|---|---|
| A | 1.77 | 104 | 0.00 | 4 |
| F = not A | 0.45 | 191 | 0.00 | 4 |
| $V_{dd}$ | 0.22 | 100 | 0.00 | 2 |
| $V_{ss}$ | 0.23 | 90 | 0.00 | 2 |

Table-7: Node parasitic properties of High speed Inverter Layout

## 8. Conclusion

A low power**,** high-speed static combinational logic circuits layouts are fabricated successfully in 90nm technology. Functionality of each logic circuit is checked and results are verified. Even though real VLSI designs exhibit a variety of logic gates and circuits, earlier work has analysis of inverter (NOT gate). In this paper we showed that the how the node parameters - MOS, Capacitance, Resistance, Inductance and Clock are effected with respect to the low power and high speed values. We also determine the timing analysis of the layout. By using this same process we can develop other custom devices. And this paper is also useful to learn how to layout design for beginners.

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